ZZSOP07AA Type

Ultra-low Offset Voltage Operational Amplifier

Product Introduction

The ZZSOP07AA ultra-low offset voltage operational amplifier circuit complies with the quality control standards of GJB597B-2012 (General Specifications for Semiconductor Integrated Circuits) and GJB548B-2005 (Test Methods and Procedures for Microelectronic Devices), achieving National Military Standard Grade B. Custom-grade Grade S products are available upon request.

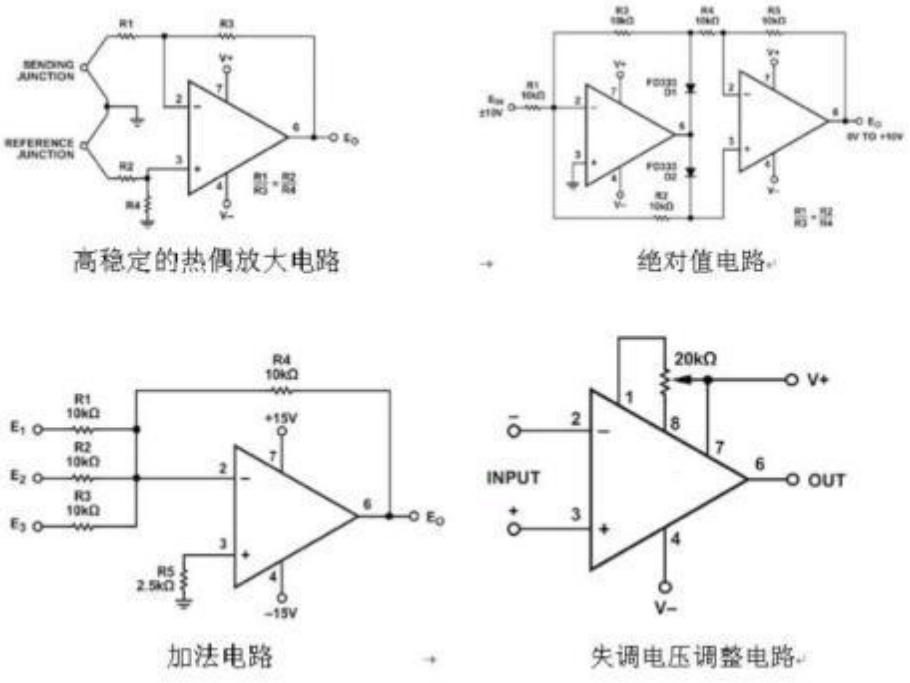
Product Technical Advantages:

- Ultra-low offset voltage: With wafer-level calibration technology, the ZZSOP07AA achieves an offset voltage as low as 25 μV.
- Excellent temperature (time) drift and noise performance: ultra-low offset voltage temperature drift below 0.6 μV/℃; ultra-low offset voltage time drift below 1.5 μV/month; low noise performance below 0.6 μVp-p.
- The ZZSOP07AA features an external resistor for adjustable offset voltage, significantly improving circuit flexibility and ensuring consistent offset voltage across multiple circuits.
- Outstanding comprehensive performance: The amplifier features a wide operating temperature range of-55℃ to +125℃, a broad input voltage range of±13V, a common-mode rejection ratio (CMRR) of at least 106dB, and high input impedance, ensuring exceptional precision in signal amplification.
- The OP07A product, imported from abroad, is fully replaced by a complete set of pins and full functionality.

Apply

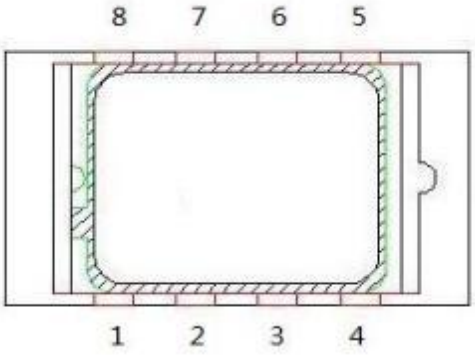
- wireless base station control circuit
- fiber optic network control circuit
- instrumentation amplifier
- Sensor and Control Thermocouple
- precision filter

Applicative Circuit



Graph 1

Introduction End Arrangement



Graph 2

Exit	Symbol	Function	Exit	Symbol	Function
1	V_{OS} TRIM	Dysregulation module	8	V_{OS} TRIM	Dysregulation module
2	−IN	Negative input terminal	7	V+	Positive power supply
3	+IN	Positive input terminal	6	V_{OUT}	Outlet end
4	V−	Negative power source	5	NC	Barefoot

Table 1 Pin Functions (Top View)

Function Declaration

The circuit logic structure diagram shall comply with the requirements specified in Figure 3.

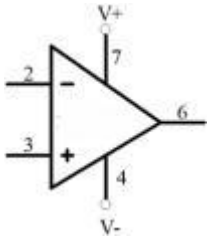


Figure 3 Circuit Logic Structure Diagram

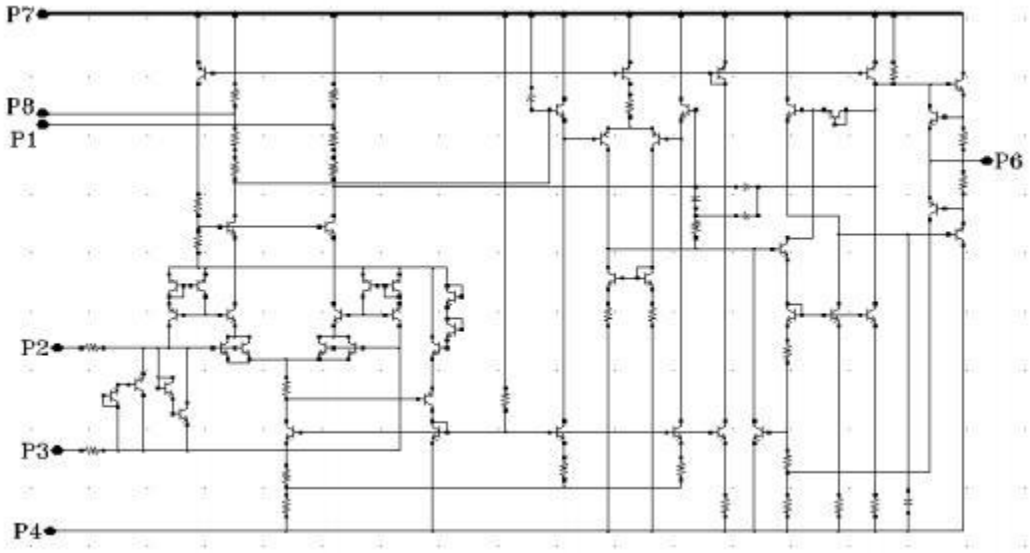
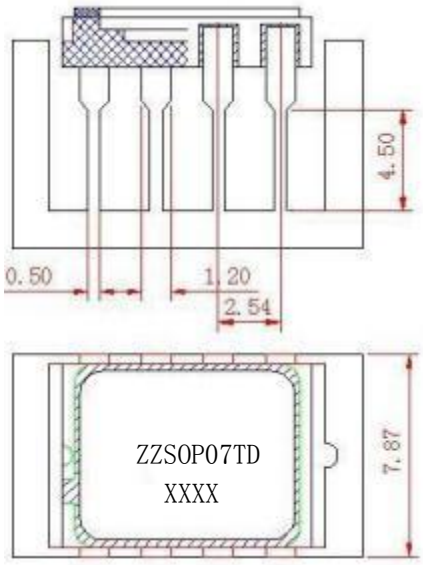


Figure 4 Internal Simplified Circuit Diagram

Encapsulation Form

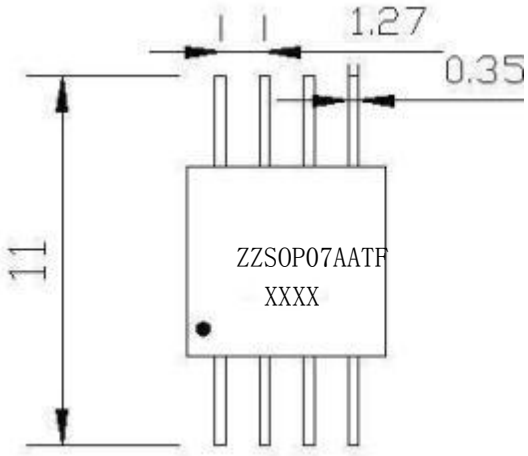
Model	Encapsulation form	Temperature range	Encapsulation size diagram
ZZSOP07TD	8 lead double row direct insertion	−55℃≤T_A≤+125℃	See Figure 5
ZZSOP07TF	8 lead ceramic flat		See Figure 6
ZZSOP07A	Provide bare die		See Figure 7
ZZSOP07A	Customize packaging based on user requirements		_

Table 2 Packaging Form Description Table



unit ：mm

Figure 5-8: Leadless Dual-Column Straight-Jam Package Dimensions



unit ：mm

Figure 6-8 Lead Ceramic Flat Package Dimensions

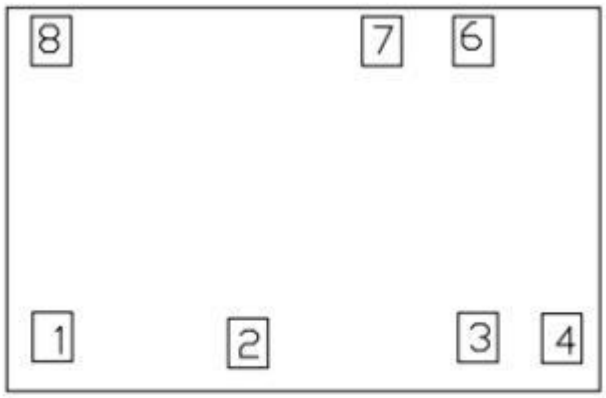


Figure 7 Schematic Diagram of Chip Size

Chip size	2.45*1.65（mm）
Weld size	100*100 （ μm）
Welding material	ALSi（Si%），1.2±0.1 μm

Table 3

Electrical Parameter Meter

Test item	Symbol	Test condition	Extreme		Unit	Temperature requirement
						−55℃≤T_A≤+125℃
			Minimum	Maximum		Unless otherwise specified
Lose balance Voltage	V_{OS}	Vs=±15V	−25	25	μV	T_A=25℃
			−60	60		
Lose balance Current	I_{OS}	Vs=±15V	−2	2	nA	T_A=25℃
			−4	4		
Input bias current （ same-phase ）	I_{B+}	Vs=±15V	−2	2	nA	T_A=25℃
			−4	4		
Input bias current （opposition ）	I_{B-}	Vs=±15V	−2	2	nA	T_A=25℃
			−4	4		
Open loop voltage gain	A_{VO}	Vs=±15V	300	—	V/mV	T_A=25℃
			200	—		
Cmrr	CMRR	Vs=±15V	110	—	dB	T_A=25℃
			106	—		
Positive power supply Pressure suppression ratio	PSRR+	Vs=±3V~±18V	—	10	μV/V	T_A=25℃
			—	20		
Negative power supply Pressure suppression ratio	PSRR−	Vs=±3V~±18V	—	10	μV/V	T_A=25℃
			—	20		
Output	VO+	RL=10K	12.5	—	V	T_A=25℃

Test item	Symbol	Test condition	Extreme		Unit	Temperature requirement
						−55℃≤T_A≤+125℃
			Minimum	Maximum		Unless otherwise specified
Voltage						
Output voltage	VO−	RL=10K	—	−12.5	V	T_A=25℃
Output voltage	VO+	RL=2K	12	—	V	
Output voltage	VO−	RL=2K	—	−12	V	
Quiescent dissipation	PS	Vs=±15V	—	120	mW	
Quiescent dissipation	PS	Vs=±3V	—	6	mW	
Swing rate	SR+	Vs=±15V	0.1	—	V/ μS	T_A=25℃
Swing rate	SR−	Vs=±15V	0.1	—	V/ μS	T_A=25℃

Table 4 Electrical Characteristics Table of ZZSOP07AA

Precautions for Circuit Use

1. The Limit Working Condition of Circuit and the Attention to It

Name	Extreme	Explain
Power Supply Voltage (VCC)	±22V	
Input voltage (VIN)	±V_{CC}	
Range of differe-ntial input voltage	±30V	If the differential input voltage exceeds ±0.7V, the input current must be limited to ±10mA.
Output short circuit duration	Infinite length	The voltage (Vs) should be ±15V, and the temperature (TA) should be 25°C. Both temperature and supply voltage must be controlled to ensure they do not exceed the rated power.
Pin temperature	+300℃	Welding duration <60 seconds.
Storage temperature range	−65℃~+150℃	
Junction temperature（TJ）	+175℃	For short-term testing (168 hours in specific aging and steady-state life test configurations), TJ = +175° C.
Maximum dissipation power（P_D）	500mW	The maximum power consumption is at ambient temperature of 25℃.
Core bonding	–	Increase the bonding wire arc radius to prevent short-circuiting between the bonding wire and the chip groove area. Automatic bonding is recommended, with a wire diameter of 25 μm.
Coreless package	–	The moisture content should be controlled according to the national military standard, with a recommended level of<1000 PPM.

Table 5

Note that exceeding the absolute maximum rated values listed above may cause permanent damage to the device. These are merely emphasized rated values and do not involve functional operation of the device under these or any other conditions beyond the technical specifications. Long-term operation at absolute maximum rated values may affect the reliability of the device.

2. **ESD Warn**

The ZZSOP07AA circuit is classified as an ESD (Electrostatic Discharge) sensitive component. Electrostatic charges can readily accumulate on both human bodies and testing equipment, potentially discharging unnoticed. Although this product incorporates a dedicated ESD protection circuit with an anti-static capability of up to 2000V, permanent device damage may occur during high-energy electrostatic discharge events. Therefore, implementing appropriate ESD mitigation measures is recommended to prevent performance degradation or functional loss of the components.

3. Recommended Operating Conditions

Power supply voltage range: ±3V to ±20.0V.

Operating environment temperature: -55℃ to +125℃.

Physical Image