

## ZZSAD62Z0

### High Precision Instrumentation Amplifier

#### Performance features

- The gain adjustment is convenient: the gain range is 1~10000 by an external resistance.
- Excellent DC performance
  - The voltage imbalance can be as low as 50  $\mu\text{V}$  (maximum).
  - Input offset drift: 0.6  $\mu\text{V}/^\circ\text{C}$  (maximum value)
- Wide voltage range:  $\pm 2.3\text{V}$  to  $\pm 18\text{V}$
- Wide operating temperature range:  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$
- Design of discrete instrumentation amplifier with performance higher than 3 operational amplifier

#### Product Introduction

The ZZSAD62Z0 instrumentation amplifier circuit complies with quality control standards specified in GJB597 B-2012 General Specifications for Semiconductor Integrated Circuits and GJB548C-2021 Testing Methods and Procedures for Microelectronic Devices, achieving National Military Standard Grade B certification. Custom Grade S products are available upon customer request and can fully replace foreign counterparts of identical models.

Table 1 Comparison With Imported Product Models

Shanzhan model	ADI model name
ZZSAD620	AD620

#### operational principle

The circuit logic structure diagram shall comply with the specifications in Figure 1. The ZZSAD62Z0 is a low-cost, high-precision instrumentation amplifier that requires only one external resistor for gain adjustment, with a gain range of 1 to 10000.

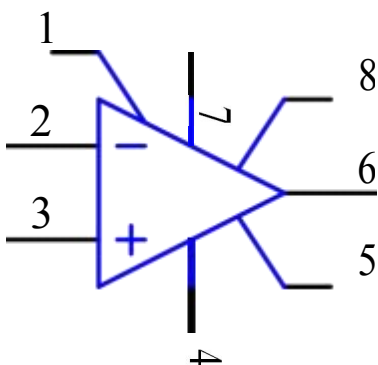


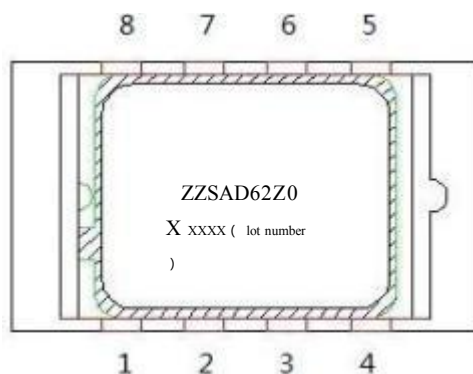
Figure 1 Circuit Logic Structure Diagram

## Performance Index

**Table 2 Electrical Characteristics of ZZSAD62Z0**

Test item	Symbol	Test condition	Extreme		Unit	Temperature requirement
			Minimum	Maximum		$-55^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$
Gain error		$V_{cc} = \pm 15\text{V}$ , $G=100$	-0.5	0.5	%	$T_A=25^{\circ}\text{C}$
Offset voltage	$V_{os}$	$V_{cc} = \pm 15\text{V}$	-125	125	$\mu\text{V}$	$T_A=25^{\circ}\text{C}$
			-185	185		
Offset current	$I_{os}$	$V_{cc} = \pm 15\text{V}$	-2.5	2.5	nA	$T_A=25^{\circ}\text{C}$
			-5.0	5.0		
Enter the bias current (in-phase)	$I_{B+}$	$V_{cc} = \pm 15\text{V}$	-5	5	nA	$T_A=25^{\circ}\text{C}$
			-7.5	7.5		
Enter the bias current (inverted)	$I_{B-}$	$V_{cc} = \pm 15\text{V}$	-5	5	nA	$T_A=25^{\circ}\text{C}$
			-7.5	7.5		
Cmrr	CMRR	$V_{cc} = \pm 15\text{V}$	110	—	dB	$T_A=25^{\circ}\text{C}$
Supply voltage rejection ratio	PSRR	$V_{cc} = \pm 3\text{V} \sim \pm 18\text{V}$	110	—	dB	$T_A=25^{\circ}\text{C}$
Output voltage	VO+	RL=10K	13.6	—	V	$T_A=25^{\circ}\text{C}$
		$V_{cc} = \pm 15\text{V}$	13.5	—	V	
Output voltage	VO-	RL=10K	—	-13.6	V	$T_A=25^{\circ}\text{C}$
		$V_{cc} = \pm 15\text{V}$	—	-13.4	V	
Quiescent current	IS+	$V_{cc} = \pm 15\text{V}$ , RL=2k	—	1.3	mA	$T_A=25^{\circ}\text{C}$
		$V_{cc} = \pm 15\text{V}$ , RL=2k	—	1.6	mA	
	IS-	$V_{cc} = \pm 15\text{V}$ , RL=2k	-1.3	—	mA	$T_A=25^{\circ}\text{C}$
		$V_{cc} = \pm 15\text{V}$ , RL=2k	-1.6	—	mA	

## Pin Description



Exit	Symbol	Function	Exit	Symbol	Function
1	Rg	Gain configuration terminal	8	Rg	Gain configuration terminal
2	-IN	Negative input terminal	7	V+	Positive power supply
3	+IN	Positive input terminal	6	V <sub>OUT</sub>	Outlet end
4	V-	Negative power source	5	REF	Reference pin

Figure 2: Pin Arrangement and Functions (top View)

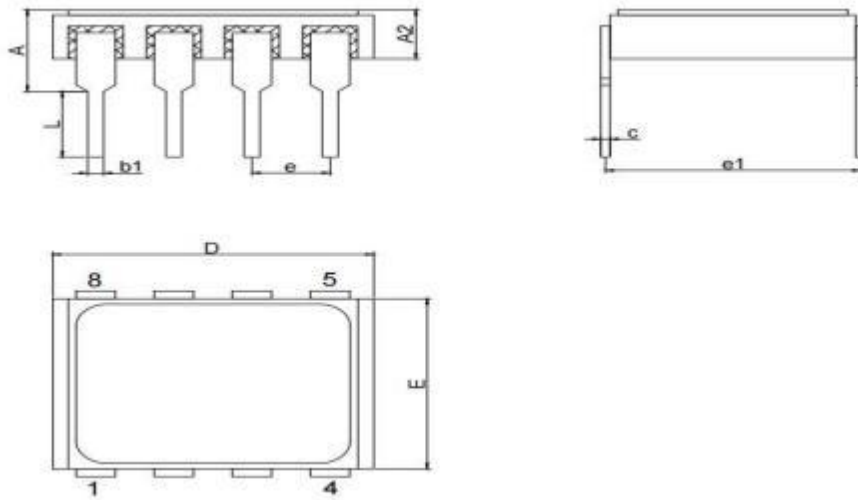
## Encapsulation and Dimensions

Model	Specifications	Encapsulation form	Encapsulation size diagram
ZZSAD62Z0	ZZSAD62Z0TD	CDIP8	See Figure 3
	ZZSAD62Z0TS	CSOP8	See Figure 4
	ZZSAD62Z0TF	CFP8	See Figure 5
	ZZSAD62Z0TM	CFP8	See Figure 6

Table 3 Packaging Form Description Table

### 8-Pin Ceramic Dual Row Direct Insertion Package

The Package Type Is CDIP8, and Its External Dimensions Must Comply With the Specifications in Figure 3.



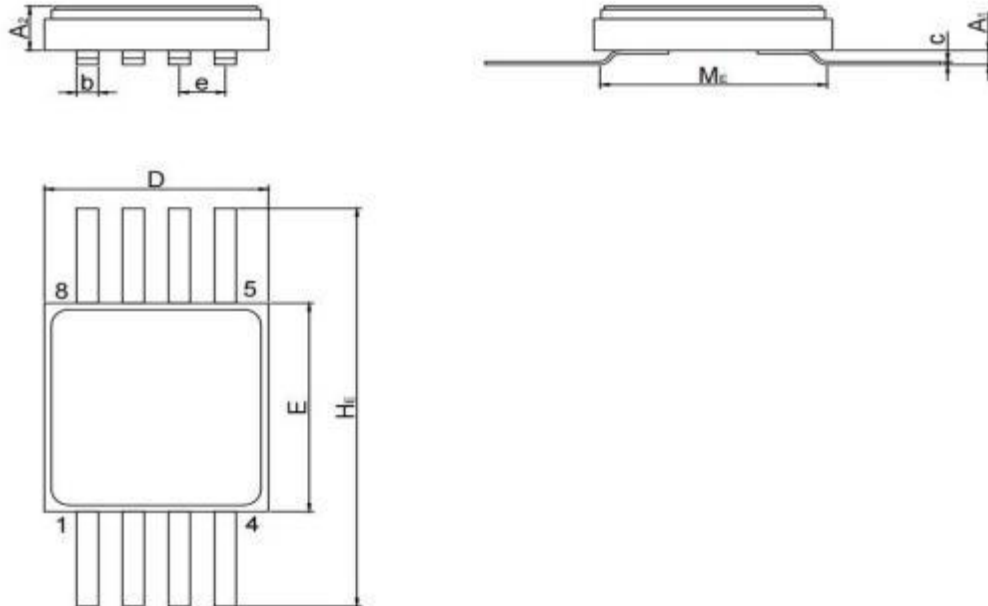
Size Symbol	Numeric value			Unit
	Minimum	Nominal	Maximum	
A			5.08	mm
A2			2.80	mm
b <sub>1</sub>	0.36		0.66	mm
c	0.20		0.36	mm
D	9.76		10.24	mm
E	7.00		7.80	mm
e		2.54	-	mm
e <sub>1</sub>		7.62	-	mm
L	2.54		5.00	mm

Note: The L size can be customized with ribbed reinforcement as required by the user.

Figure 3.8 Outline drawing of 8-lead ceramic dual in-line package

## 8 Lead Ceramic Small Package

The Packaging Shall Be CSOP8, With Dimensions Conforming to Figure 4.



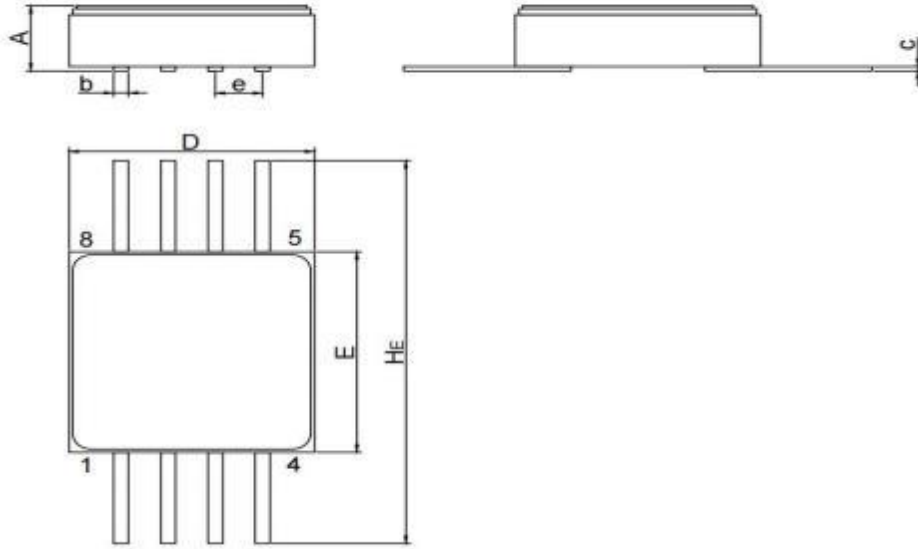
Dimension Symbol	Numeric value			Unit
	Minimum	Nominal	Maximum	
A <sub>1</sub>			1.60	mm
A <sub>2</sub>			2.00	mm
b	0.20		0.60	mm
c	0.10		0.35	mm
D	5.79		6.21	mm
E	6.19		6.61	mm
e		1.27	-	mm
H <sub>E</sub>	8.40		16.70	mm
M <sub>E</sub>	5.50		6.10	mm

Note: H<sub>E</sub> and A<sub>1</sub> dimensions can be customized for rib cutting and reshaping according to user requirements, and the reshaping is performed before delivery.

Figure 4.8 Outline drawing of 8-lead ceramic small outline package

## 8-Pin Ceramic Flat Package

The Packaging Shall Be CFP8, With Dimensions Conforming to Figure 5.



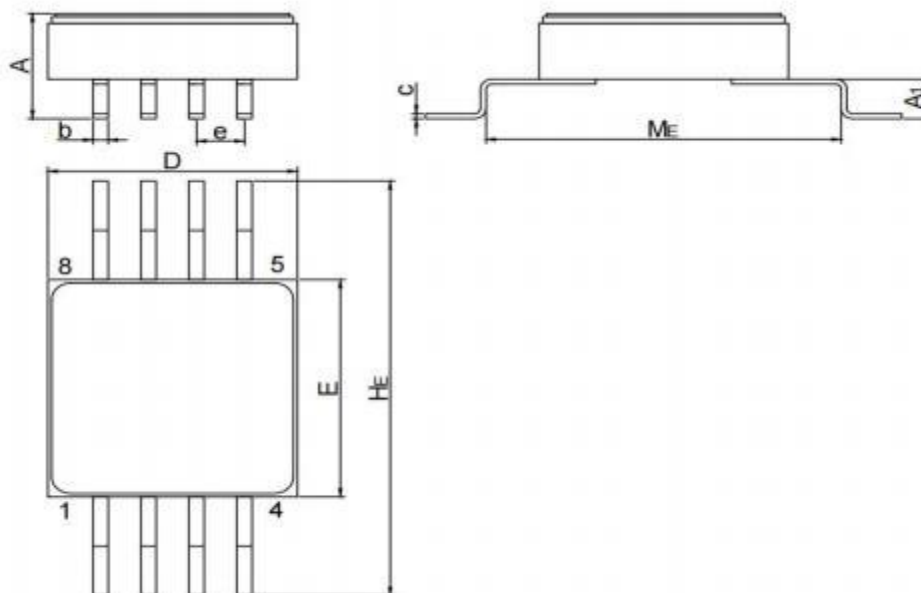
Size Symbol	Numeric value			Unit
	Minimum	Nominal	Maximum	
A	1.80		2.20	mm
b	0.35		0.45	mm
c	0.10		0.20	mm
D	6.36		6.64	mm
E	6.36		6.64	mm
e		1.27	-	mm
HE	10.50		11.50	mm

Note: The HE size can be customized with ribbed reinforcement as required, and the final shaping is completed prior to delivery.

Figure 5. Outline drawing of 8 Lead Ceramic Flat Package

## 8 Lead Flat Bend Lead Ceramic Package

The packaging shall be CFP8, with dimensions conforming to Figure 6.



Dimension Symbol	Numeric value			Unit
	Minimum	Nominal	Maximum	
A			4.00	mm
A1 <sup>a</sup>			2.00	mm
b	0.35		0.45	mm
C	0.10		0.20	mm
D	6.36		6.64	mm
E	6.36		6.64	mm
e		1.27		mm
HE	10.90		11.50	mm
ME <sup>a</sup>	8.00		8.80	mm

<sup>a</sup> The dimensional accuracy of the external shape is guaranteed by the manufacturing equipment and shall not be used as a basis for inspection; moreover, the shaping process is performed prior to delivery.

Figure 6 8 Lead Ceramic Flat Bend Lead Package Shape

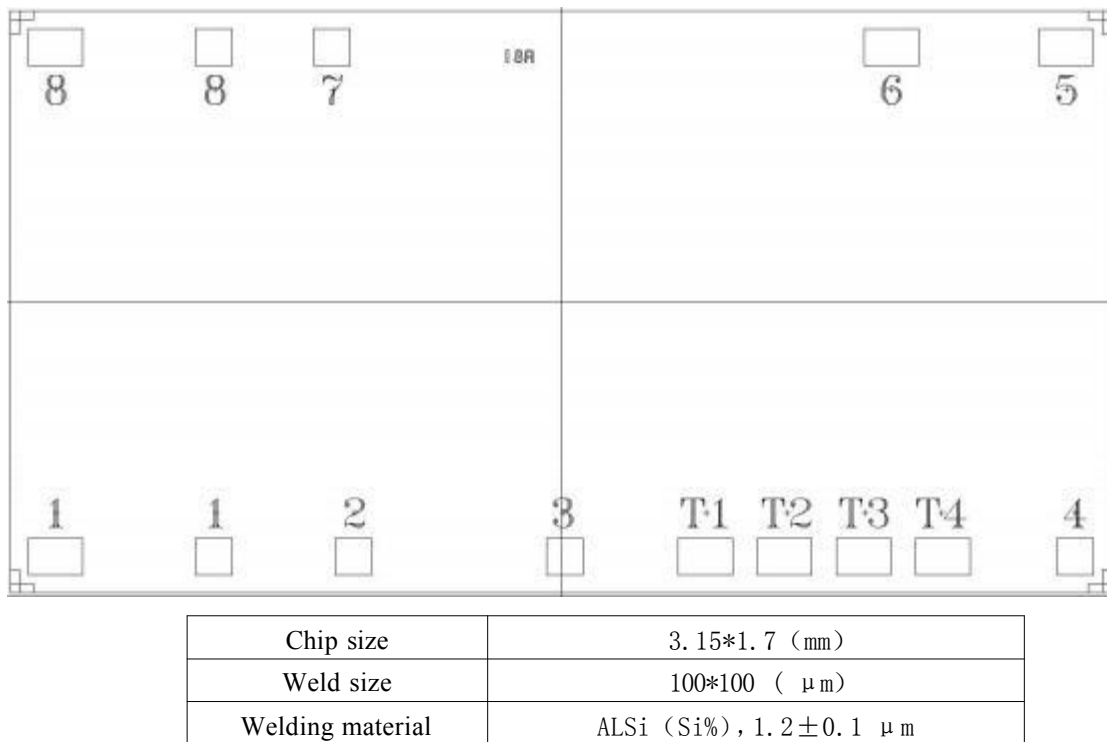


Figure 7 Schematic diagram of chip size

**Typical applications**

- 1. medical instruments
- 2. sensor interface
- 3. data acquisition system
- 4. industrial process control
- 5. Battery-powered portable device

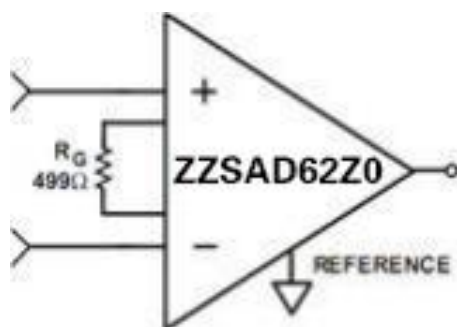


Figure 8 Typical Application Diagram

## Other

### (1) Circuit Limit Operating Conditions and Precautions

Name	Extreme	Explain
Power supply voltage ( $V_{cc}$ )	$\pm 18V$	
Input voltage ( $V_{IN}$ )	$V_{cc}$	
Range of differential input voltage	25V	
Pin temperature	+300°C	Welding duration <10 seconds.
Storage temperature range	-65°C to +150°C	Tao Feng
	-55°C to +125°C	Plastic package
Operating temperature range	-55°C to +125°C	
Maximum dissipation power ( $P_D$ )	650mW	The maximum power consumption is at ambient temperature of 25°C.

Table 4

Note: Exceeding the absolute maximum rated values listed above may cause permanent damage to the device. These are merely emphasized ratings and do not cover functional operation under these or any other conditions beyond the technical specifications. Prolonged operation at absolute maximum rated values may affect the device's reliability.

### (II) ESD Warning

The ZZSAD62Z0 circuit is an ESD-sensitive component. Static charges can easily accumulate on both human bodies and test equipment, potentially discharging unnoticed. Although this product features a dedicated ESD protection circuit with a withstand voltage of up to 2000V, permanent device damage may occur when exposed to high-energy electrostatic discharge. Therefore, it is recommended to implement appropriate ESD protection measures to prevent performance degradation or functional loss of the device.

