AASW606AQ

2.4 GHz WLAN Front-End Module

Features

- Integrated 802.11ax, 2.4 GHz PA, LNA with bypass, and T/R switch
- Fully-matched input and output
- Integrated logarithmic power detector and directional coupler
- Transmit gain: 33 dB
- Receive gain: 14 dB
- Output power:
- MCS11, +21 dBm, -43 dB EVM
- MCS9, +22.5 dBm, -35 dB EVM
- MCS7, +23.5 dBm, -30 dB EVM
- Small QFN (16-pin, 3 x 3 mm) package (MSL3, 260℃ per JEDEC J-STD-020)

Applications

- 802.11ax set-top boxes, networking, and personal computer systems
- PC cards, PCMCIA cards, mini-cards, and half mini-cards
- WLAN enabled wireless video systems

Description

The AASW606AQ is a highly integrated, 2.4 GHz front-end module (FEM) incorporating a 2.4 GHz single-pole, double-throw (SPDT) transmit/receive (T/R) switch, a 2.4 GHz low-noise amplifier (LNA) with bypass, and a

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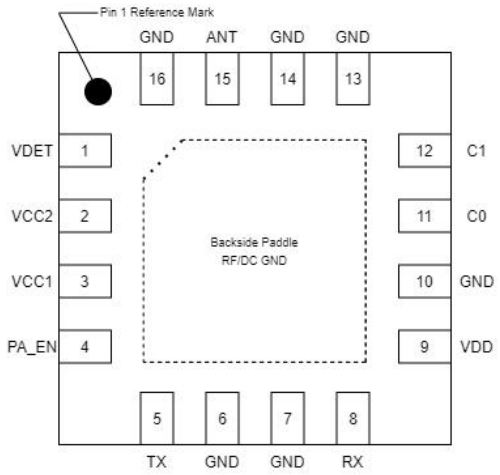
2.4 GHz power amplifier (PA) intended for mobile/portable 802.11ax applications and systems.

An integrated power detector is included to provide closed-loop power control within the system.

The device is provided in a compact, 16-pin 3 x 3 mm Quad Flat No-Lead (QFN) package.

Functional Block Diagram



Ordering Information

- GSW606AQ

Recommended Operating Conditions

Parameter		Symbol	Units	Min	Typ	Max
Supply Voltage		VCC1、VCC2、VDD	V	—	5.0	—
Control Logic	VIH	PA_EN、C0、C1	—	—	—	—
	VIL	PA_EN、C0、C1	—	—	—	—
Operational Frequency Range		—	GHz	2.4	—	2.5
Operating Temperature		—	℃	-40	—	85

Absolute Maximum Ratings

Parameter		Symbol	Units	Min	Typ	Max
Supply Voltage		VCC1、VCC2、VDD	V	-0.3	—	6
Control Logic	VIH	PA_EN、C0、C1	V	1.5	—	3.6
	VIL	PA_EN、C0、C1	V	0	—	0.6
RF Input Power (Pin), CW, 50ohms, T=25℃		RX、TX、ANT	dBm	—	—	10
Storage Temperature		—	℃	-60	—	150
ESD Rating	HBM	—	V	—	1000	—
	CDM	—	V	—	1000	—

Electrical Specifications

Test Conditions: 50Ω system, VCC=VDD=5V, Temp=+25℃, (de-embedded data);

Parameter	Symbol	Test Condition	Units	Min	Typ	Max
Frequency range	f	Main frequency band	GHz	2.4	—	2.5
Transmit Mode						
Gain	G	—	dB	32.6	33	33.4
Gain flatness	ΔG	Over any 40 MHz band	dB	-0.4	—	0.4
Output power	POUT	DEVM = -43 dB, MCS11, HE40	dBm	—	21	—
		DEVM = -40 dB, MCS10, HE40	dBm		22	
		DEVM = -35 dB, MCS9, VHT40	dBm		22.5	
		DEVM = -30 dB, MCS7, HT20	dBm		23.5	
		802.11b, HT20 mask compliant	dBm		27	
Current consumption	I_{TOT}	@ +27 dBm	mA	—	475	—
		@ +24 dBm	mA		378	
		@ +20 dBm	mA		301	
		@ +18 dBm	mA		275	
2nd harmonics	2fo	+25 dBm MCS0	dBm/MHz	—	-11	—
3rd harmonics	3fo	+25 dBm MCS0	dBm/MHz	—	-35	—
non-harmonic spurious	—	+25 dBm MCS0	dBm/MHz	—	-50	—
Isolation	—	From ANT to RX, State 4	dB	—	50	—
Input return loss	|S11|	—	dB	—	13	—
Output return loss	|S22|	—	dB	—	7	—
Power detector output	VDET	@ No RF	v	—	0.37	—
		@ +5 dBm	v	—	0.38	—
		@+11 dBm	v	—	0.43	—

		@ +26 dBm	v	—	0.75	—
Power detector slope	SLOPE	From +13 to +26 dBm	mV/dB	—	20	—
Power detector error	ERR_{DET}	From +13 to +26 dBm	dB	-1.5	—	1.5
Power detector output impedance	Z_{OUT}_DET	RF output = -30 dBm	Ω	—	10K	—
—	I_{ENABLE}	—	mA	—	0.50	—
Stability	STAB	POUT = +25 dBm, VCC = 5 V, 64 QAM, 6:1 VSWR, all phases	—		none	
Ruggedness	Ru	Maximum input power, 10:1 mismatch, no permanent damage	dBm	—	—	10

Parameter	Symbol	Test Condition	Units	Min	Typ	Max
Frequency range	f	Main frequency band	GHz	2.4	—	2.5
Receive Mode						
Gain	G	LNA active LNA bypass	dB dB	—	14.2 -8.6	—
1 dB input compression point	IP1dB	LNA active LNA bypass	dBm dBm	—	-1 20	—
Gain step	—	—	dB	—	22.8	—
Gain flatness	—	Over any 40 MHz	dB	-0.1	—	0.1
Noise figure	NF	—	dB	—	1.6	—
Input return loss	|S11|	LNA active LNA bypass	dB dB	—	15 15	—
Output return loss	|S22|	LNA active LNA bypass	dB dB	—	12 20	—
Third order input intercept point	IIP3	—	dBm	—	10	—
Switching time	t_{SW}	LNA<-> bypass	ns		200	

		RX<->TX: From 10%-> 90% power change of rising or falling edge	ns		450	
LNA bias current	I_{DD}	—	mA	—	30	—
C0, C1 current	—	—	μA	—	10	—

Control Logic

Mode	State	C0	C1	PA_EN
All off (switch in TX mode)	1	0	0	0
WLAN receive	2	1	0	0
WLAN receive bypass mode	3	1	1	0
WLAN transmit (high-linearity mode)	4	0	1	1

AASW606AQ

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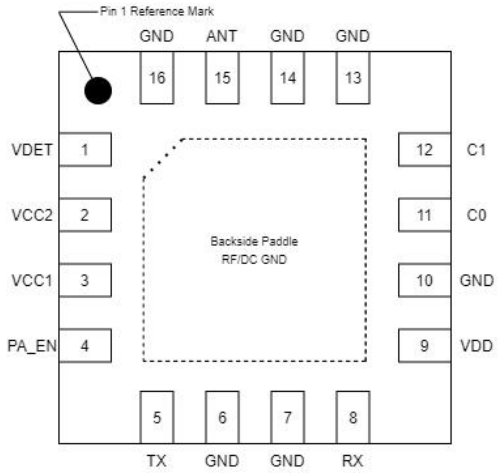
Pin Assignments and Description



Pin	Name	Description	Pin	Name	Description
1	VDET	Detector output	9	VDD	LNA supply
2	VCC2	PA supply	10	GND	Ground
3	VCC1	PA supply	11	C0	Control logic
4	PA_EN	PA enable	12	C1	Control logic
5	TX	RF transmit input	13	GND	Ground
6	GND	Ground	14	GND	Ground
7	GND	Ground	15	ANT	Antenna
8	RX	RF receive output	16	GND	Ground

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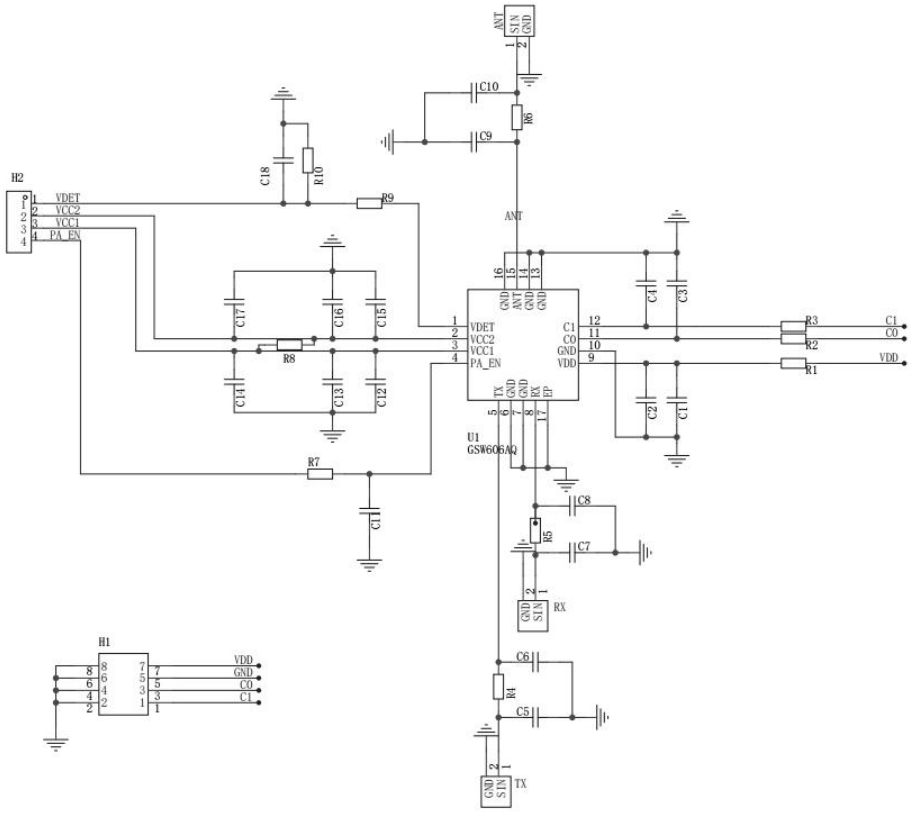
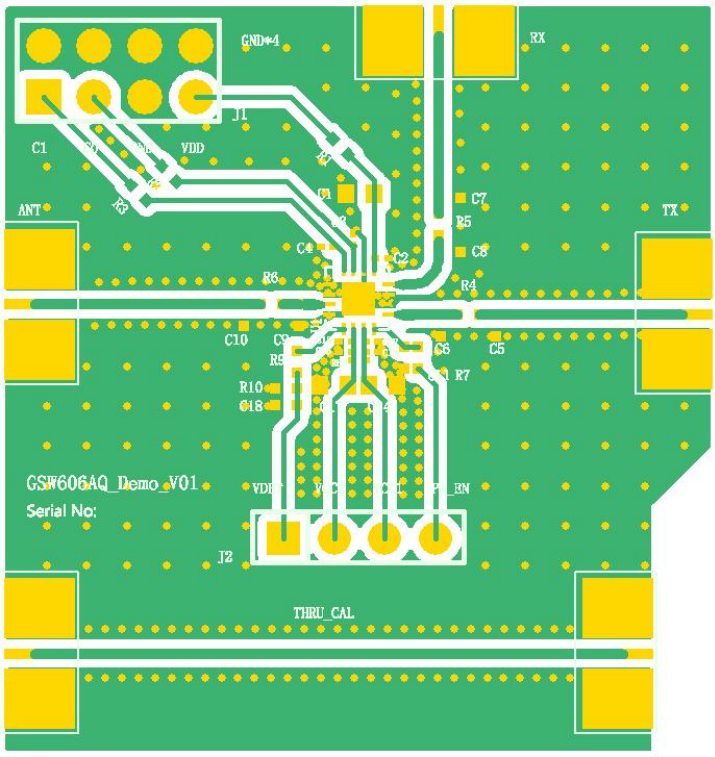
PCB Evaluation Board





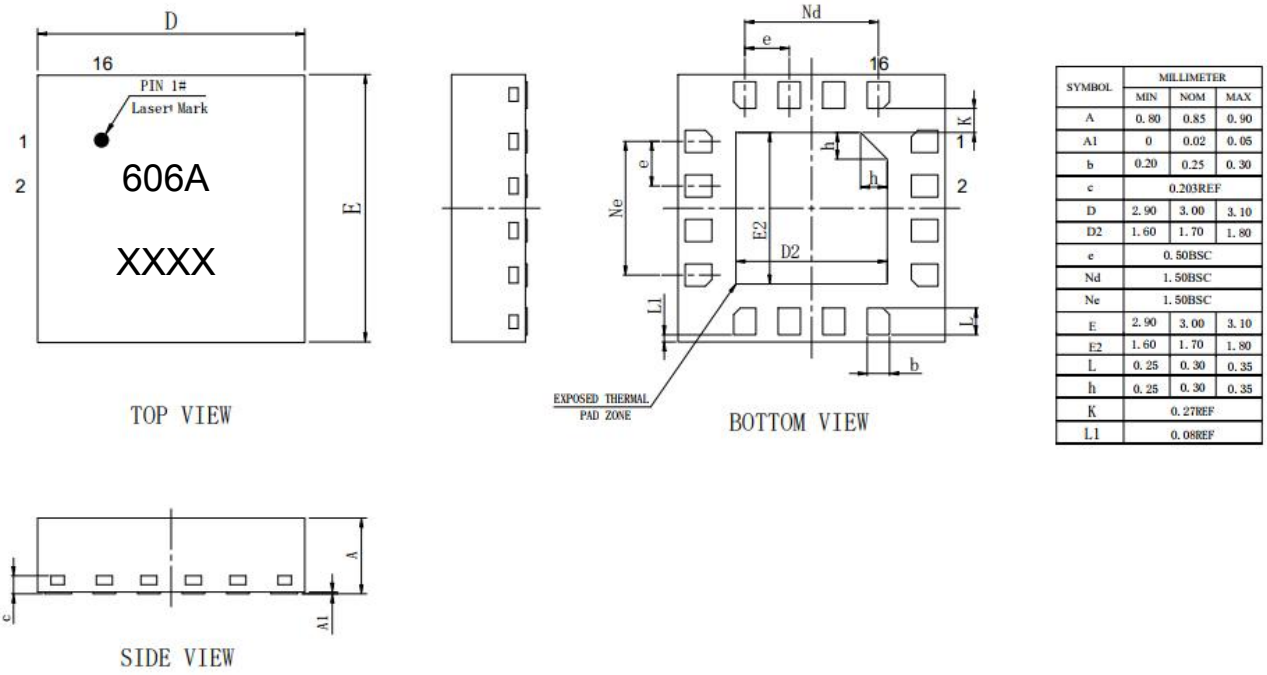
Evaluation Board BOM

Reference Des.	Conditions	Value	Manuf.	Part Num.
PCB	N/A	N/A	SDSX	GSW606AQ-Demo-V01
U1	N/A	N/A	SDSX	GSW606AQ
C12、C15	N/A	220pF	MuRata	0201
C3、C4	N/A	2.2uF	MuRata	0201
C2	N/A	100pF	MuRata	0201
C5、C6	N/A	300Ω	MuRata	0402
C16、C13	N/A	1nF	MuRata	0201
C18	N/A	100nF	MuRata	0402
C9、C10、C11、C8、C7、R10、R8	N/A	NA	MuRata	N/A
C17、C1、C14	N/A	10uF	MuRata	0603
R4	N/A	16Ω	MuRata	0402
R1、R2、R3、R5、R6、R7、R9	N/A	0R	MuRata	0402

Package Marking and Dimensions

Marking: Part number – 606A

Lot code – XXXX



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0	0.02	0.05
b	0.20	0.25	0.30
c	0.203REF		
D	2.90	3.00	3.10
D2	1.60	1.70	1.80
e	0.50BSC		
Nd	1.50BSC		
Ne	1.50BSC		
E	2.90	3.00	3.10
E2	1.60	1.70	1.80
L	0.25	0.30	0.35
h	0.25	0.30	0.35
K	0.27REF		
L1	0.08REF		

Notes: 1. All dimensions are in millimeters.

2. Coplanarity applies to the exposed heat sink slug as well as the terminals.

3. QFN 16 pin 3x3x0.85mm Package.

Handling Precaution

ESD countermeasure methods should be developed and used to control potential ESD damage during handling in a factory environment at each manufacturing site.

Solderability

Compatible with lead-free (260 ℃ maximum reflow temperature) soldering processes.

RoHS Compliance

This product is compliant with the EU RoHs2.0, EU Directive 2015/863.

Revision history

Document ID	Release date	Data sheet status	Change notice
V1.0	20220331	Preliminary	• Initial version.
V1.1	20220401	Preliminary	• Updated Electrical Specifications • Updated Evaluation Board BOM