ZZZSOP177 Type
Ultra-low Offset Operational Amplifier

Summary

The ZZZSOP177 ultra-low offset operational amplifier is manufactured in compliance with the ' GJB597B-2012 General Specifications for Semiconductor Integrated Circuits' and 'GJB548B-2005 Test Methods and Procedures for Microelectronic Devices' standards, achieving a National Military Standard Class B quality rating. Custom Class S products are available upon customer request.

Product Technical Advantages:

- Ultra-low offset voltage: With wafer-level calibration technology, the ZZZSOP177 achieves an offset voltage as low as 25 μ V.
- Excellent temperature (time) drift and noise performance: ultra-low offset voltage temperature drift below 0.1 μV/℃; below 1.5 μV/month ultra-low drift voltage with sub-0.6 μVp-p low noise performance.
- A convenient method for adjusting offset voltage: The ZZZSOP77A features an external resistance connection to regulate offset voltage, significantly enhancing circuit flexibility and ensuring consistent offset voltage across multiple circuits.
- Outstanding comprehensive performance: -Wide operating temperature range from-55℃ to +125℃, ±13 V input voltage range, common-mode rejection ratio (CMRR) of ≥130dB, power supply voltage rejection ratio (PSRR) of ≥115dB, linear gain of ≥5000V/mV, and power consumption below 60mW.
- The OP177 product replaces imported foreign OP177 models with full-pin configuration and comprehensive performance, while maintaining pin compatibility with OP77A models.

Apply

- wireless base station control circuit
- fiber optic network control circuit
- instrumentation amplifier
- Sensor and Control Thermocouple
- precision filter

Introduction End Arrangement

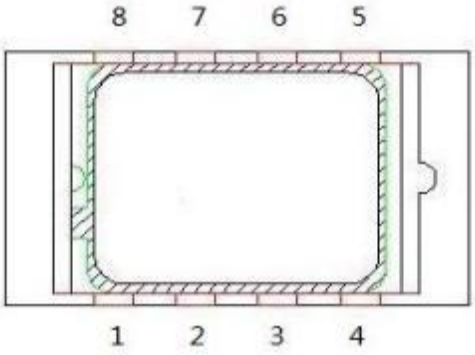


Figure 1: Input Port Arrangement

Exit	Symbol	Function	Exit	Symbol	Function
1	V_{OS} TRIM	Dial adjustment terminal	8	V_{OS} TRIM	Dial adjustment terminal
2	-IN	Negative input terminal	7	V+	Positive power supply
3	+IN	Positive input terminal	6	V_{OUT}	Outlet end
4	V-	Negative power source	5	NC	Barefoot

Table 1 Pin Functions (Top View)

Function Declaration

The circuit logic structure diagram shall comply with the requirements specified in Figure 2.

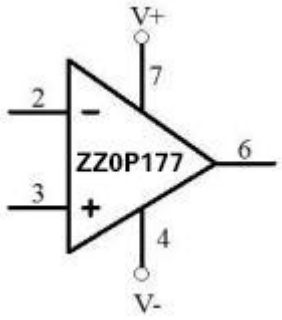


Figure 2 Circuit Logic Structure Diagram

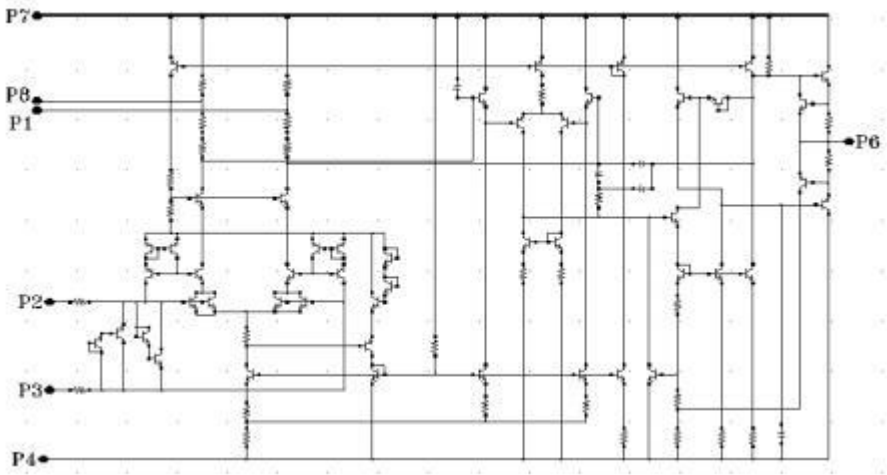
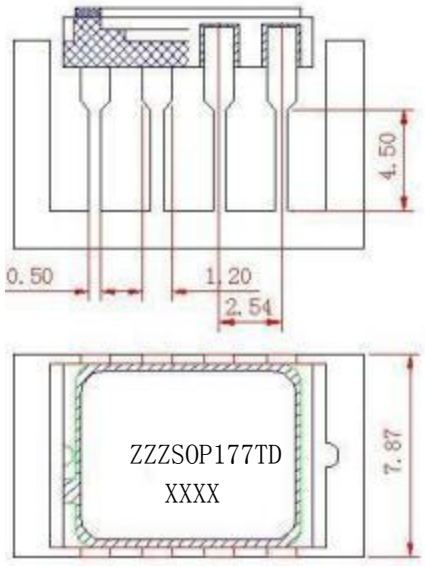


Figure 3 Internal Simplified Circuit Diagram

Package Description

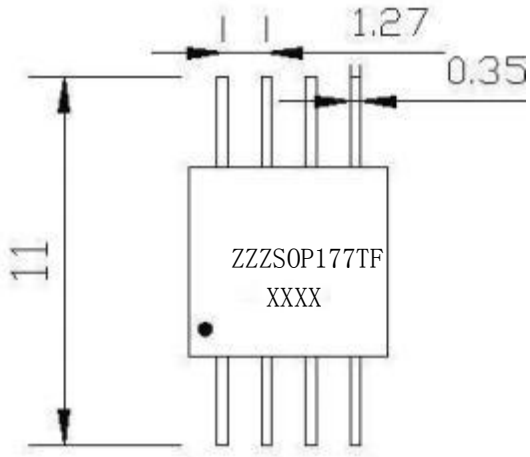
Table 2 Packaging Form Description Table

Model	Encapsulation form	Temperature range	Encapsulation size diagram
ZZSOP177TD	8 Dual-row lead-through connector	−55℃≤T_A≤+125℃	See Figure 4
ZZSOP177TF	8 lead ceramic flat		See Figure 5
ZZZSOP177	Provide bare die		See Figure 6
ZZZSOP177	Customize packaging based on user requirements		_



unit： mm

Figure 4-8: Leadless Dual-Column Straight-Jam Package Dimensions



unit： mm

Figure 5-8 Lead Ceramic Flat Package Dimensions

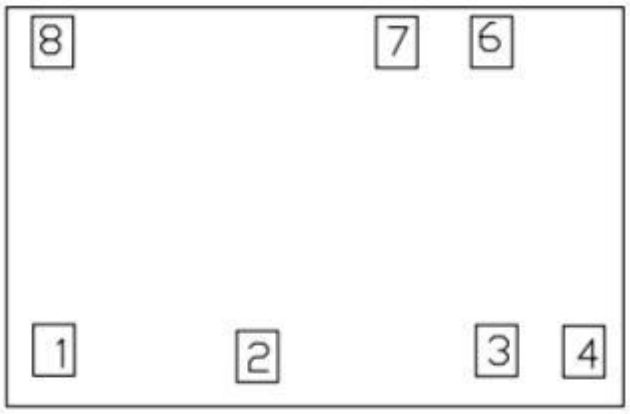


Figure 6 Schematic Diagram of Chip Size

Chip size	2.45*1.65（mm）
Weld size	100*100 （ μm）
Welding material	ALSi（Si%），1.2±0.1 μm

Table 3

Electrical Parameter Meter

Test item	Symbol	Test condition	Extreme		Unit	Temperature requirement
						-55℃≤T_A≤+125℃
			Minimum	Maximum		Unless otherwise provided
Offset voltage	V_{OS}	Vs=±15V	-25	25	μV	T_A=25℃
			-40	40		
Offset current	I_{OS}	Vs=±15V	-1.5	1.5	nA	T_A=25℃
			-2.2	2.2		
Input bias Current (in phase)	I_{B+}	Vs=±15V	-0.2	2		T_A=25℃
			-0.2	4	nA	
Input bias Current (inverted)	I_{B-}	Vs=±15V	-0.2	2	nA	T_A=25℃
			-0.2	4		
Open loop voltage gain	A_{VO}	Vs=±15V	5000	—	V/mV	T_A=25℃
			2000	—		
Cmrr	CMRR	Vs=±15V	130	—	dB	T_A=25℃
			120	—	dB	
Positive power supply Pressure suppression ratio	PSRR+	Vs=±3V~±18V	—	1.5	μV/V	
Negative power supply	PSRR-	Vs=±3V~±18V	—	1.5	μV/V	

Test item	Symbol	Test condition	Extreme		Unit	Temperature requirement
						$-55℃ \leqslant T_A \leqslant +125℃$
			Minimum	Maximum		Unless otherwise provided
Pressure suppression ratio						
Output voltage	VO+	RL=10K	13.5	—	V	T_A=25℃
Output voltage	VO−	RL=10K	—	−13.5	V	T_A=25℃
Output voltage	VO+	RL=2K	12.5	—	V	T_A=25℃
			12	—	V	
Output voltage	VO−	RL=2K	—	−12.5	V	T_A=25℃
			—	−12	V	
Quiescent dissipation	PS	Vs=±15V	—	60	mW	T_A=25℃
			—	75	mW	
Quiescent dissipation	PS	Vs=±3V	—	4.5	mW	T_A=25℃
Swing rate	SR+	Vs=±15V	0.1	—	V/ μS	T_A=25℃
Swing rate	SR−	Vs=±15V	0.1	—	V/ μS	T_A=25℃

Table 4 Electrical Characteristics ofZZZSOP177

Precautions for Circuit Use

1. The Limit Working Condition of Circuit and the Attention to It

Name	Extreme	Explain
Power Supply Voltage (VCC)	±22V	
Input voltage (VIN)	$\pm V_{CC}$	
Range of differential input voltage	±30V	If the differential input voltage exceeds ±0.7V, the input current must be limited to ±10mA.
Output short circuit duration	Infinite length	The voltage (Vs) should be ±15V, and the temperature (TA) should be 25°C. Both temperature and supply voltage must be controlled to ensure they do not exceed the rated power.
Pin temperature	+300℃	Welding duration <60 seconds.
Storage temperature range	−65℃~+150℃	
Junction temperature （TJ）	+175℃	For short-term testing (168 hours in specific aging and steady-state life test configurations), TJ = +175℃.
Maximum dissipative power (PD)	500mW	The maximum power consumption is at ambient temperature of 25℃.
Core bonding	–	Increase the bonding wire arc radius to prevent short-circuiting between the bonding wire and the chip groove area. Automatic bonding is recommended, with a wire diameter of 25 μm.
Coreless package	–	Control moisture content during encapsulation according to national military standards, recommended <1000 PPM

Table 5

Note: Exceeding the absolute maximum rated values listed above may cause permanent damage to the device. This is only

The emphasized rated values do not cover functional operations of the device exceeding these or any other specified conditions. Prolonged operation at absolute maximum rated values may compromise the device's reliability.

2. **ESD Warn**

The ZZZSOP177 circuit is ESD-sensitive. Static charges can easily accumulate on both human bodies and test equipment, potentially discharging unnoticed. Although this product features a dedicated ESD protection circuit with a withstand voltage of up to 2000V, permanent device damage may occur during high-energy static discharge. Therefore, implementing appropriate ESD protection measures is recommended to prevent performance degradation or functional loss.

3. Recommended operating conditions

Power supply voltage range: ±3V to ±20.0V;

Working environment temperature: -55°C to +125°C.

Physical Image Display