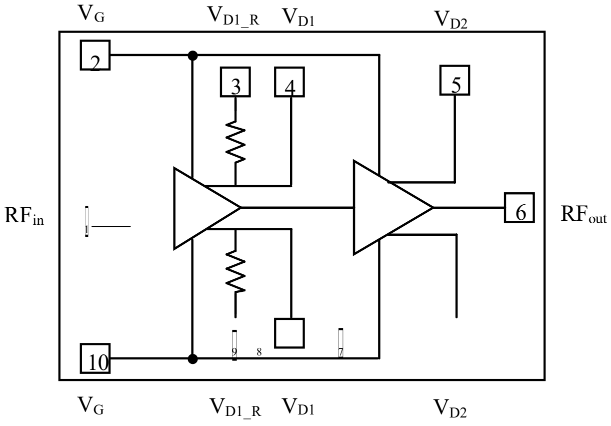
HX116752C-405P40 GaN MMIC **power amplifier chip,**4.0GHz～5.0GHz

Performance Features

- Frequency range: 4.0 GHz to 5.0 GHz
- Power gain: 25dB
- Maximum output power: 46dBm
- Power added efficiency: 53%
- +28V@0.9A (static)
- Chip dimensions: 3.5mm × 3.4mm × 0.08mm

functional block diagram



Product Overview

The HX116752C-405P40 is a high-power amplifier chip implemented using GaN HEMT transistors, fabricated through GaN power MMIC technology. Operating within a frequency range of 4.0GHz to 5.0GHz, it delivers a power gain of 25dB, a typical saturated output power of 40W, and a typical power add-on efficiency of 53%, with compatibility for both pulse and continuous wave modes. The chip features backside via grounding and dual power supply operation, with typical operating voltages of Vd=+28V and Vg=-2.4V. It is primarily applied in microwave transceiver components and solid-state transmitters.

DC current parameters (TA = +25℃)

Metric	Symbol	Least value	Representative value	Crest value	Unit
Gate operating voltage	Vg	-2.6	-2.4	-2.2	V
Drain operating voltage	Vd	-	28	-	V
Static drain current	Id	-	0.8	-	A
Dynamic drain current	Idd	-	3	3.7	A
Dynamic gate current	Igg	-	1	10	mA

Microwave electrical parameters (TA = +25°C, Vd = +28V, Vg = -2.4V)

Metric	Symbol	Least value	Representative value	Crest value	Unit
Frequency range	f	4.0～5.0			GHz
Saturated output power	Psat	45.5	46		dBm
Power gain	Gp	24.5	25		dB
Power gain flatness	△Gp			±1	dB
Power added efficiency	PAE	50	53		%
Linear gain	Gain	29	31	33	dB
Linear gain flatness	△Gain			±1.0	dB
Input standing wave	VSWR(in)		2.0	2.5	-

Note: 1) All chips have undergone in-chip 100% DC testing and 100% RF testing.

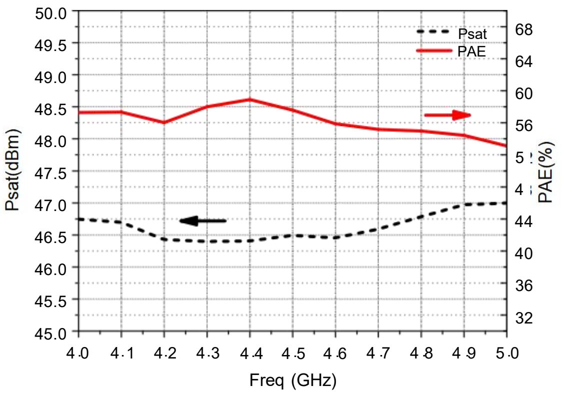
2) Unless otherwise specified, the curve test conditions in this manual are: Vd=+28V, Vg=-2.4V, Pin=21dBm, pulse width 100μs, and duty cycle 10%.

Limit usage parameters

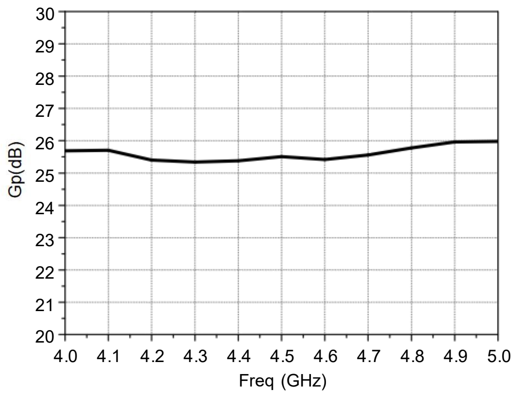
Parameter	Symbol	Limit value
Maximum drain-source voltage	Vd	+36V
Maximum gate-source voltage	Vg	-3.5V
Maximum input power (CW)	P_p	+26dBm
Storage temperature	T_{STG}	-65℃～+150℃
Maximum operating channel temperature	T_{op}	+200℃
Load impedance mismatch (anti-burnout)	Z_0	5:1

Typical curve (Vg=-2.3V, Vd=+28V, pulse width 100μs, duty cycle 10%)

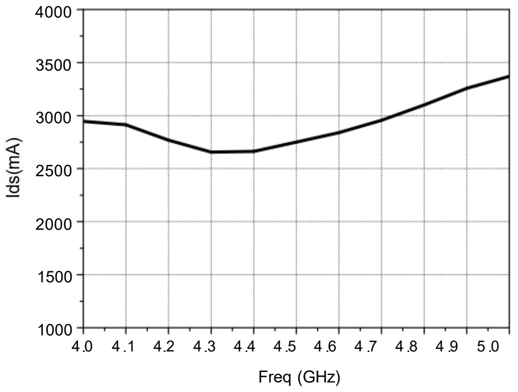
Maximum output power/efficiency versus frequency (Pin=21dBm)



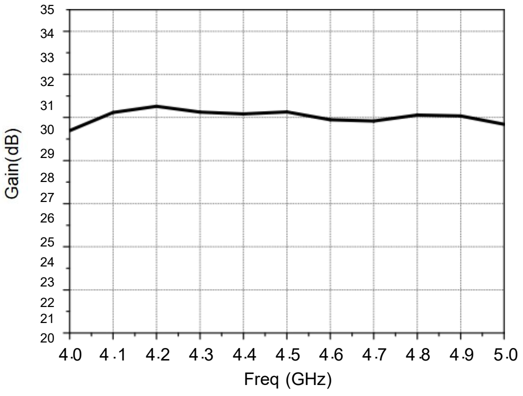
Power gain vs. frequency (Pin=21dBm)



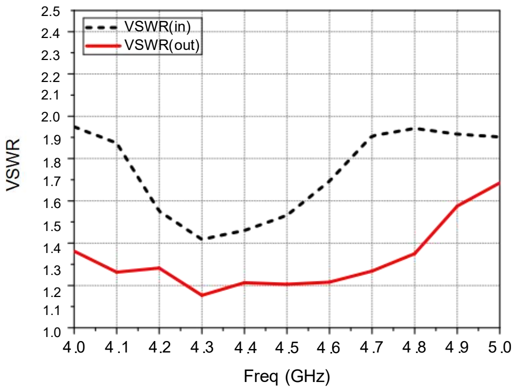
Dynamic drain current vs. frequency (Pin=21dBm)



Small signal gain vs. frequency (Pin=-10dBm)

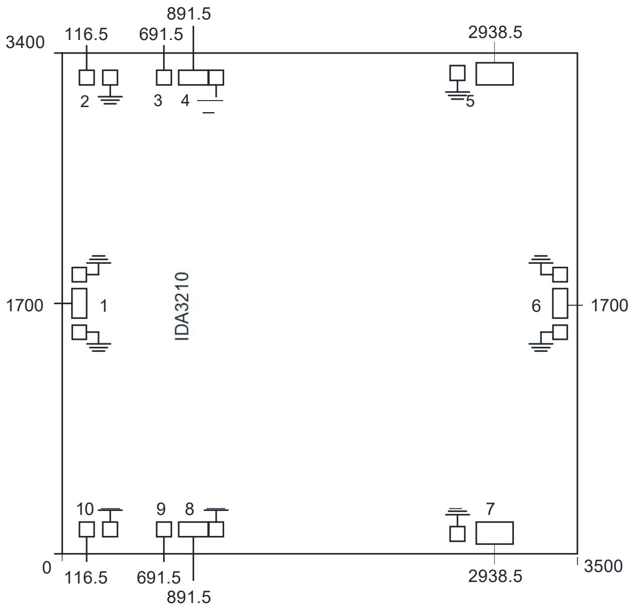


Standing wave vs. frequency (Pin=-10dBm)



External dimensions and pressure point arrangement diagram

Dimensional drawing and contact arrangement diagram of HX116752C-405P40

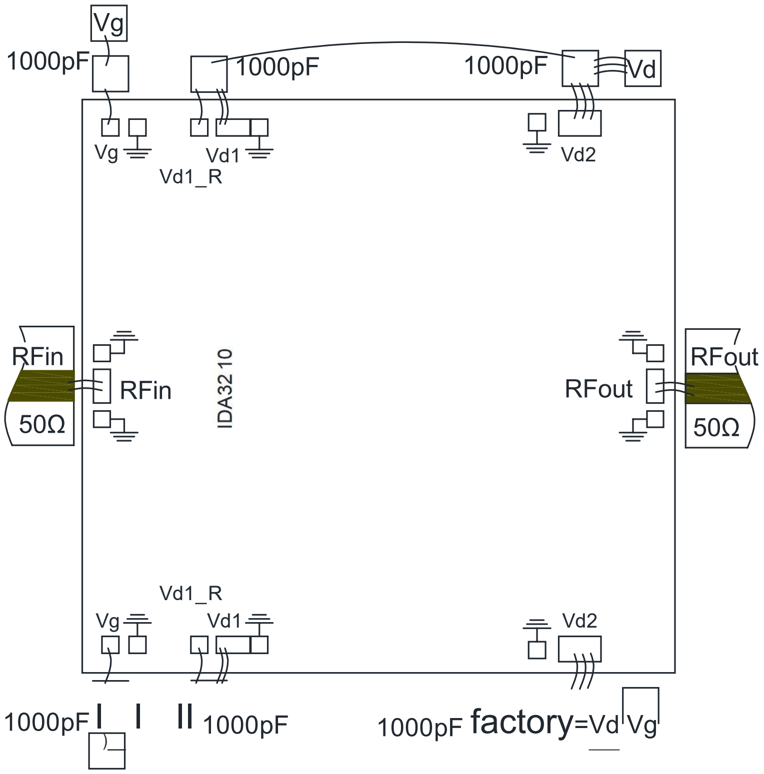


Note: All units in the figure are in micrometers (μm); dimensional tolerance ±100μm.

Pressure Point Arrangement Diagram

Serial number	Symbol	Function	Size （μm）	Coordinate （μm） x， y
1	RF_{in}	Radio frequency input pressure point	100×200	116.5， 1700
2	V_G	Level 1, Level 2 gate bonding pressure points	100×100	116.5， 3233.5
3	V_{D1_R}	First-stage drain series resistance bonding pressure point	100×100	691.5， 3233.5
4	V_{D1}	First-level drain bonding pressure point	200×100	891.5， 3233.5
5	V_{D2}	Secondary drain bonding pressure point	250×150	2938.5， 3258.5
6	RF_{out}	RF output voltage point	100×200	3383.5， 1700
7	V_{D2}	Secondary drain bonding pressure point	250×150	2938.5， 141.5
8	V_{D1}	First-level drain bonding pressure point	200×100	891.5， 166.5
9	V_{D1_R}	First-level drain series resistance bonding pressure point	100×100	691.5， 166.5
10	V_G	Level 1, Level 2 gate bonding pressure points	100×100	116.5， 166.5
Else	GND	Grounding pressure point for probe testing	100×100	

Recommended Assembly Drawing



Matters Need Attention

1） Single-chip circuits must be stored in a dry and clean nitrogen (N2) environment.

2） The chip substrate material 6H-SiC is highly brittle and must be handled with care to avoid damaging the chip.

3） The chip surface lacks an insulating protective layer, necessitating attention to the cleanliness of the assembly environment to prevent excessive surface contamination.

4） The thermal expansion coefficient of the carrier should be close to that of 6H-SiC, with a linear thermal expansion coefficient of 4.2×10^{-6}/℃. It is recommended to use CuMoCu, CuMo, or CuW as the carrier material.

5） During assembly, avoid gaps between the chip and the carrier while ensuring effective heat dissipation between the housing and the carrier.

6） It is recommended to use gold-silver solder for sintering with Au:Sn=80%:20%, where the sintering temperature should not exceed 300°C and the duration should not exceed 30 seconds. The sintering process must avoid rapid temperature fluctuations and requires gradual temperature rise and fall.

7） It is recommended to use gold wires with a diameter of 25μm to 30μm, maintain the temperature of the bonding platform base below 250°C, minimize bonding time, and avoid rapid temperature fluctuations during the bonding process.

8） During power-on, apply gate voltage before drain voltage; during power-off, first reduce drain voltage then gate voltage.

9） The chip incorporates DC-blocking capacitors for internal input/output, while both input and output interfaces feature DC-to-ground short-circuit configurations.

10）During chip usage and assembly, attention must be paid to anti-static measures, including wearing grounded anti-static wristbands and ensuring proper grounding of sintering and bonding platforms.

11）We offer QF087 type metal-ceramic tube shell packaging products.

12）Please contact the supplier if you have any questions.

This product is sensitive to static electricity. Please take anti-static precautions during use.