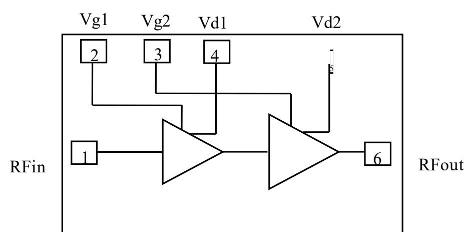
HX116744C-1428P6 S **Band amplifier,** 1.4GHz～2.8GHz

Performance Features

- Frequency range: 1.4 GHz to 2.8 GHz
- Power gain: 31dB
- Maximum output power: 39dBm
- Power added efficiency: 48%
- Chip dimensions: 4.00mm × 2.23mm × 0.10mm

functional block diagram



Product Overview

The HX116744C-1428P6 is a high-power amplifier chip operating in the S-band, implemented using GaN HEMT transistors and fabricated through GaN power MMIC technology. It covers a frequency range of 1.4GHz to 2.8GHz, featuring a power gain of 31dB, saturated output power of 39dBm, and a typical power add-on efficiency of 48%. The chip supports both pulse and continuous wave operation modes and employs backside via grounding with dual power supply configuration, maintaining typical operating voltages of Vd=+28V and Vg=-1.8~-2.0V. This device is primarily designed for microwave transceiver components and related applications.

DC current parameters (TA = +25°C)

Metric	Symbol	Least value	Representative value	Crest value	Unit
Gate operating voltage	Vg	-2.2	-1.8	-1.6	V
Drain operating voltage	Vd	24	28	32	V
Static drain current	Id		0.65		A
Dynamic drain current	Idd	0.50		0.67	A
Static gate current	Ig		1		mA
Dynamic gate current	Igg			10	mA

Microwave electrical parameters (TA = +25°C, Vd = +28V, Vg = -1.8V)

Metric	Symbol	Least value	Representative value	Crest value	Unit
Frequency range	f	1.4～2.8			GHz
Saturated output power	Psat	38.5	39		dBm
Power gain	Gp	30.5	31.0		dB
Power gain flatness	△Gp			±0.5	dB
Power added efficiency	PAE	48	50		%
Linear gain	Gain	37			dB
Linear gain flatness	△Gain			±1.5	dB
Input standing wave	VSWR(in)		2.5		-
Second harmonic				-10	dBc

Note: 1) All chips underwent in-chip 100% DC testing and 100% RF testing under the following conditions: Vd=+28V (PW=100μs, DC=10%), Vg=-1.8V.

2) Unless otherwise specified, all curves in this manual are from assembly testing conducted under the following conditions: Vd=+28V (continuous wave), pin=8 dBm; linear performance input power: Pin=-30dBm.

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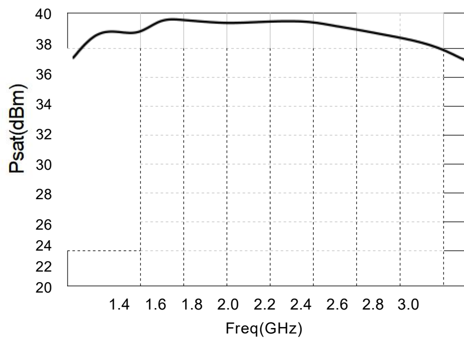
Limit usage parameters

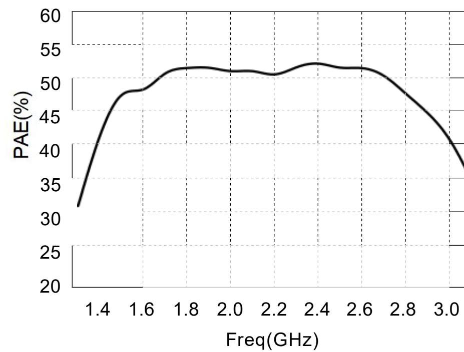
Parameter	Symbol	Limit value
Maximum drain-source voltage	Vd	+40V
Maximum gate-source voltage	Vg	-6V
Maximum input power (CW)	P_p	+14dBm
Storage temperature	T_{STG}	-65℃~+150℃
Maximum operating channel temperature	T_{op}	+225℃
Load impedance mismatch (anti-burnout)	Z_0	10:1

Typical curve (Vd=+28V, Vg=-1.8V)

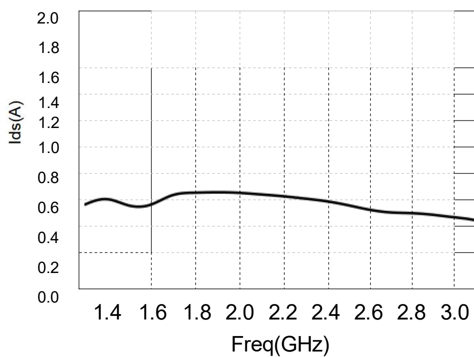
Maximum output power/efficiency versus frequency (Pin=8dBm)



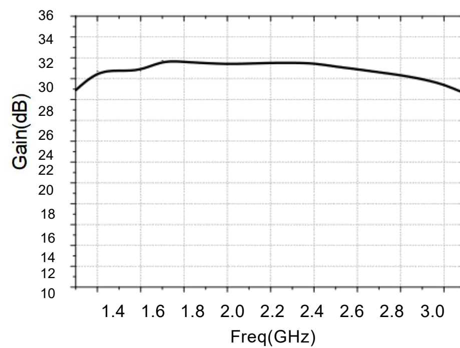
Power gain vs. frequency (Pin=8dBm)



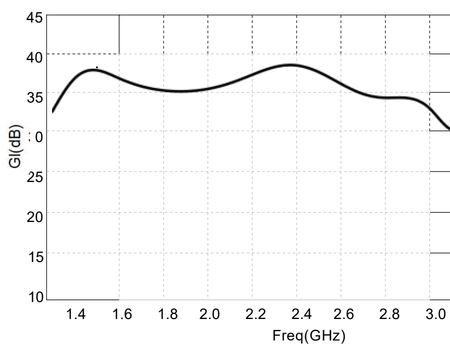
Dynamic drain current vs. frequency (P_{in}=8 dBm)



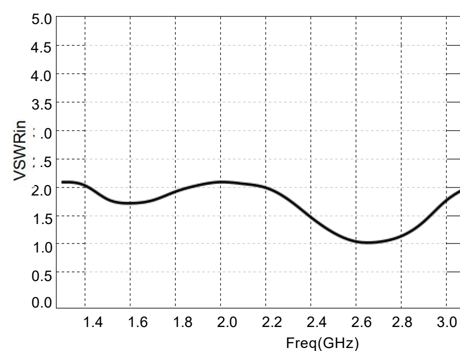
Gain vs. Frequency (P_{in}=8dBm)



Small signal gain vs. frequency (Pin=-30dBm)



Input voltage standing wave ratio vs. frequency (Pin=-30dBm)



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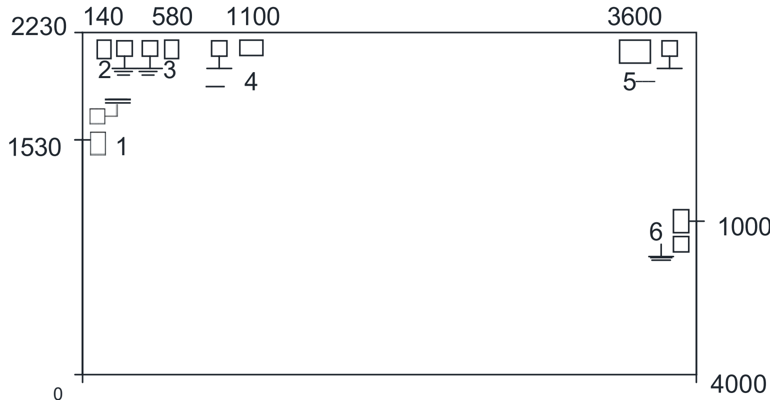
External Dimensions and Pressure Point Arrangement Diagram

External dimensions of HX116744C-1428P6

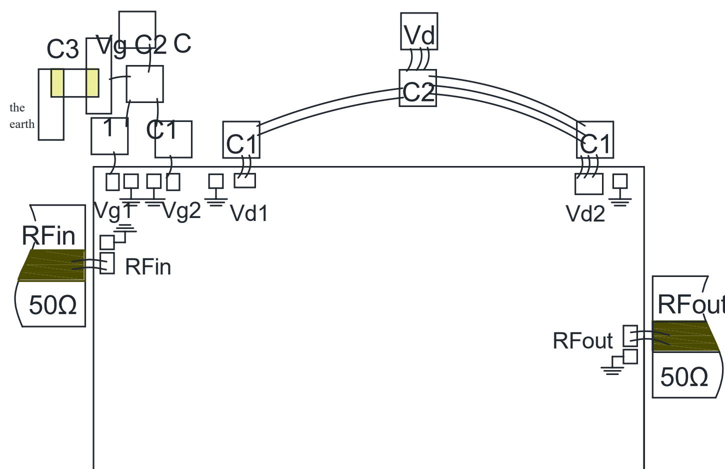


Note: All units in the figure are in micrometers (μm); dimensional tolerance ±100μm.

Pressure point arrangement diagram

Serial number	Symbol	Function	Size
1	RFin	Input pressure point	100×150μm²
2	Vg1	Gate bonding pressure point	90×120μm²
3	Vg2	Gate bonding pressure point	90×120μm²
4	Vd1	Drain bonding pressure point	150×100μm²
5	Vd2	Drain bonding pressure point	200×150μm²
6	RFout	Output pressure point	100×200μm²

Recommended Assembly Drawing



Note: 1) The capacitance values for peripheral capacitors are C1=100pF and C2=1000pF. Single-layer ceramic capacitors are recommended, with C1 positioned as close as possible to the chip and maintaining a distance of no more than 750μm.

2) For power circuits in the Ku-band and below, ceramic sintered microstrip lines with thicknesses of 200μm to 300μm can be fabricated on substrates to simplify assembly processes. For Ku-band and higher frequency bands, low-loss, low dielectric constant materials with thicknesses ranging from 125μm to 250μm are used for microstrip line bonding/sintering on substrates to reduce transmission loss, with input/output keyhole alloy wire lengths controlled within 350μm ± 150μm.

3) The gate requires a large capacitor, with C3 = 10μF.

Matters Need Attention

1） Single-chip circuits must be stored in a dry and clean nitrogen (N2) environment.

2） The chip substrate material 6H-SiC is highly brittle and must be handled with care to avoid damaging the chip.

3） The chip surface lacks an insulating protective layer, necessitating attention to the cleanliness of the assembly environment to prevent excessive surface contamination.

4） The thermal expansion coefficient of the carrier should be close to that of 6H-SiC, with a linear thermal expansion coefficient of 4.2×10^{-6}/℃. It is recommended to use CuMoCu or diamond/Cu as the carrier material.

5） During assembly, avoid gaps between the chip and the carrier while ensuring effective heat dissipation between the housing and the carrier.

6） It is recommended to use gold-silver solder for sintering with Au:Sn=80%:20%, where the sintering temperature should not exceed 300°C and the duration should not exceed 30 seconds. The sintering process should avoid rapid temperature changes and require gradual temperature rise and fall.

7） It is recommended to use gold wires with a diameter of 25μm to 30μm, maintain the temperature of the bonding platform base below 250°C, minimize bonding time, and avoid rapid temperature fluctuations during the bonding process.

8） During power-on, apply gate voltage before drain voltage; during power-off, first reduce drain voltage then gate voltage.

9） The chip incorporates DC-blocking capacitors for internal input/output, while its input terminals feature a DC-to-ground short-circuit configuration.

10）During chip usage and assembly, attention must be paid to anti-static measures, including wearing grounded anti-static wristbands and ensuring proper grounding of sintering and bonding platforms.

11）Please contact the supplier if you have any questions.

This product is sensitive to static electricity. Please take anti-static precautions during use.