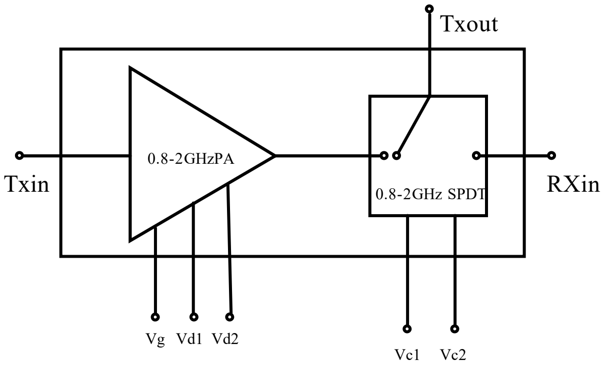
HX116790C-0820P8 GaN MMIC **power amplifier chip, 0.8GHz**～2.0GHz

Performance Features

- Frequency range: 0.8 GHz to 2.0 GHz
- Power gain: 27dB
- Maximum output power: 39.5 dBm
- Power added efficiency: 48%
- Static current: 780mA@28V; 780mA@15V; 770mA@12V
- Chip dimensions: 3.60mm × 3.20mm × 0.10 mm

functional block diagram



Product Overview

The HX116790C-0820P8 is a high-power L-band amplifier chip fabricated using GaN MMIC technology, featuring integrated transmit/receive switches. Operating within a frequency range of 0.8GHz to 2.0GHz, it delivers 27dB power gain, 39.5dBm saturated output power, and a typical power add-on efficiency of 48%, with compatibility for both pulse and continuous-wave modes. The chip employs backside via grounding for electrical isolation. The amplifier section operates on dual power supplies, with typical operating parameters including drain bias voltage Vd=+28V and **gate bias voltage** Vg=-1.8 to-2.0V. Switching functionality is achieved through adjustable negative voltage control (-28V to-40V/0V), enabling seamless switching between transmit and receive paths. This chip is primarily designed for microwave transceiver components and related applications.

DC current parameters (TA = +25℃)

Metric	Symbol	Least value	Representative value	Crest value	Unit
Gate operating voltage	Vg	-2.2	-1.8	-1.6	V
Drain operating voltage	Vd	-	28	32	V
Static drain current	Id		0.63		A
Dynamic drain current	Idd	-	0.65	0.67	A
Static gate current	Ig		1		mA
Dynamic gate current	Igg		5	-	mA
Switching control voltage	VC1/VC2		0		V
		-40		-20	V

Microwave electrical parameters I (TA = +25°C, Vd = +28V, Vg = -1.8V, VC1 = -28V, VC2 = 0V)

Metric	Symbol	Least value	Representative value	Crest value	Unit
Frequency range	f	0.8～2.0			GHz
Saturated output power	Psat	39.5	40		dBm
Power gain	Gp	26.5	27		dB
Power gain flatness	△Gp			±0.5	dB
Power added efficiency	PAE	48	50		%
Linear gain	Gain			36	dB
Linear gain flatness	△Gain			±1.5	dB
Input standing wave	VSWR(in)		2.0		-

Microwave Electrical Parameters II (TA = +25°C, Vd = +15V, Vg = -1.8V, VC1 = -28V, VC2 = 0V)

Metric	Symbol	Least value	Representative value	Crest value	Unit
Frequency range	f	0.8～2.0			GHz
Saturated output power	Psat	35.2	35.5	-	dBm
Power gain	Gp	22.0	22.5	-	dB
Power gain flatness	△Gp			±0.4	dB
Power added efficiency	PAE	43	47		%
Input standing wave	VSWR(in)		2.0		-

Microwave electrical parameters III (TA = +25°C, Vd = +12V, Vg = -1.8V, VC1 = -28V, VC2 = 0V)

Metric	Symbol	Least value	Representative value	Crest value	Unit
Frequency range	f	0.8～2.0			GHz
Saturated output power	Psat	33.8	34.4	-	dBm
Power gain	Gp	20.8	21.4	-	dB
Power gain flatness	△Gp			±0.4	dB
Power added efficiency	PAE	40	45		%
Input standing wave	VSWR(in)		2.0		-

Microwave electrical parameters IV (TA = +25°C, VC1 = 0V, VC2 = -28V)

Metric	Symbol	Least value	Representative value	Crest value	Unit
Frequency range	f	0.8～2.0			GHz
Receiving switch loss	IL	-0.6			dB

Note: 1) All chips underwent in-chip 100% DC testing and 100% RF testing under the following conditions: Vd=+28V (PW=100 μ s, DC=10%), Vg=-1.8V.

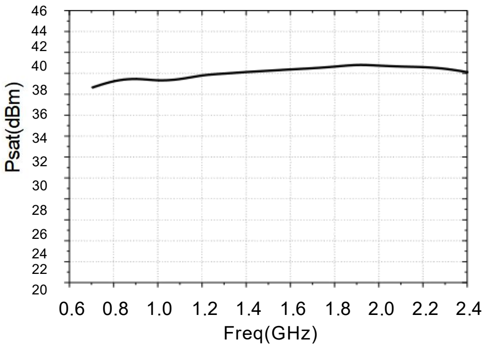
2）Unless otherwise specified, all curves in this manual are from assembly testing under the following conditions: Vd=+28V (continuous wave), pin= 8dBm; linear index input power: Pin=-30dBm;

usage restriction parameters

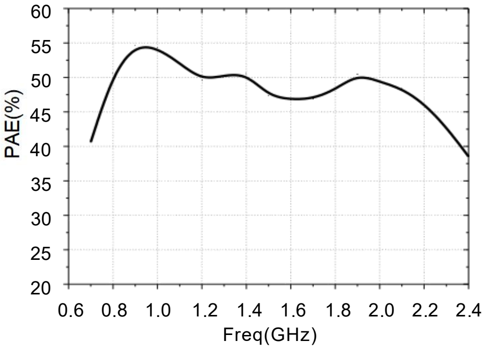
Parameter	Symbol	Limit value
Maximum drain-source voltage	Vd	+40V
Maximum gate-source voltage	Vg	-6V
Maximum input power (CW)	P_p	+16dBm
Storage temperature	T_{STG}	-65℃~+150℃
Maximum operating channel temperature	T_{op}	+200℃
Load impedance mismatch (anti-burnout)	Z_0	10:1

Typical curve I (Vd=+28V, Vg=-1.8V, VC1=-28V, VC2=0V)

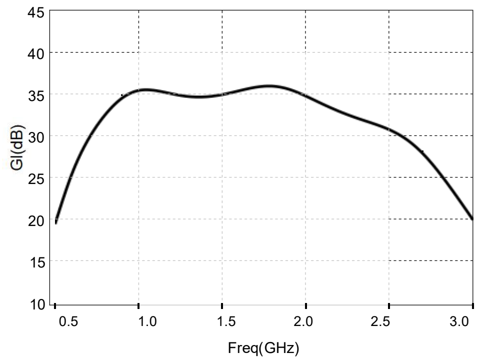
Maximum output power vs. frequency (Pin = 13dBm)



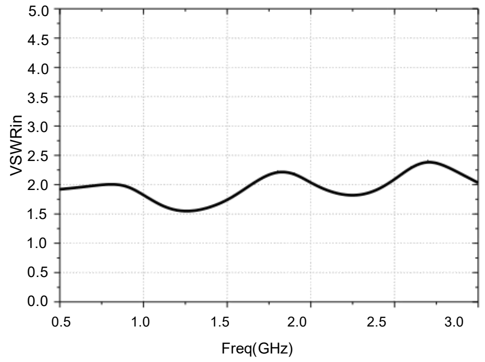
Power additive efficiency vs. frequency (P_{in}= 13dBm)



Small signal gain versus frequency (Pin=-30dBm)

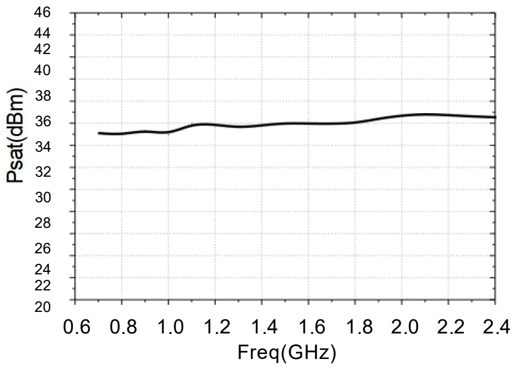


Input voltage standing wave ratio vs. frequency (P_{in}=-30dBm)

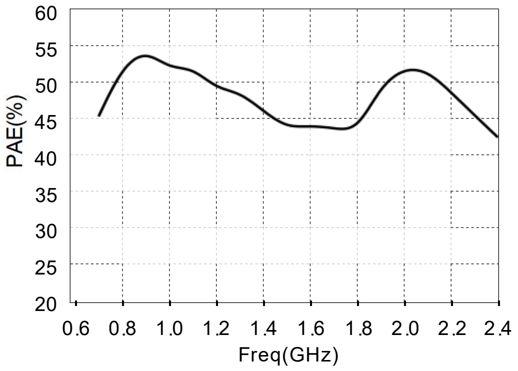


Typical curve II (Vd=+15V, Vg=-1.8V, VC1=-28V, VC2=0V)

Saturation output power vs. frequency (P_{in}= 13dBm)

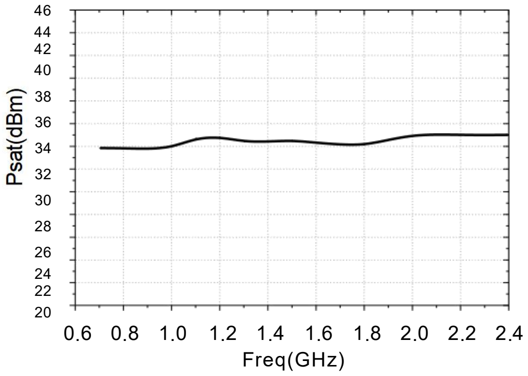


Power added efficiency versus frequency (Pin = 13 dBm)

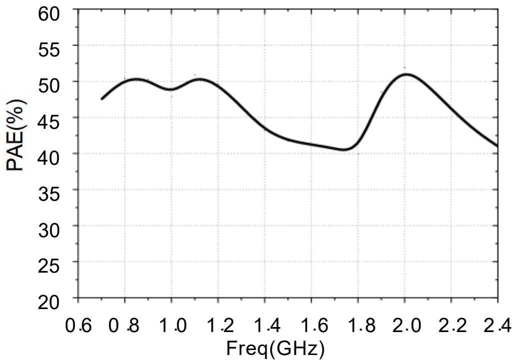


Typical curve III (Vd=+12V, Vg=-1.8V, VC1=-28V, VC2=0V)

Saturation output power/efficiency vs. frequency (Pin = 13dBm)

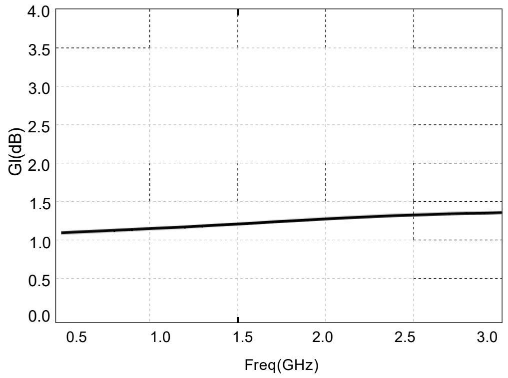


Power added efficiency versus frequency (Pin = 13 dBm)

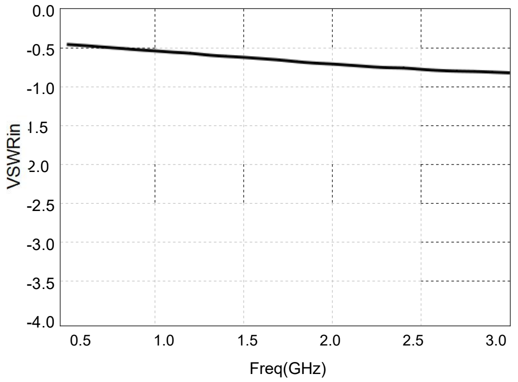


Typical curve IV (VC1=0V, VC2=-28V)

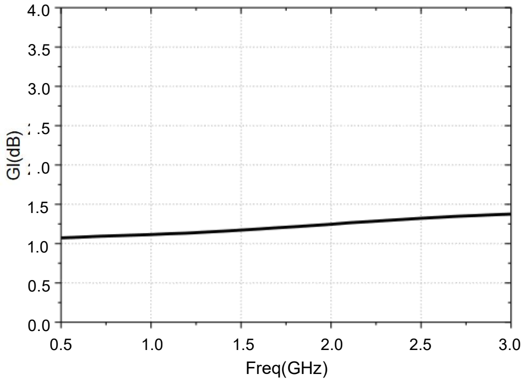
Input voltage standing wave ratio vs. frequency (Pin=-30dBm)



Switch receiving loss vs. frequency (P_{in}= -30dBm)

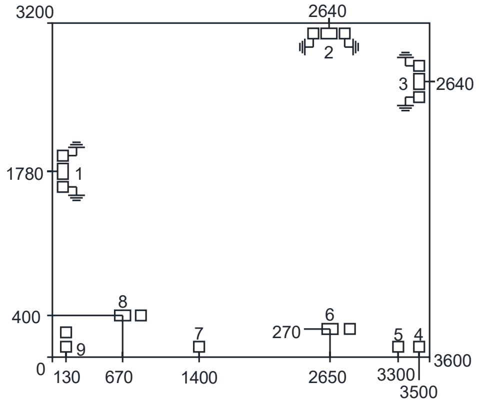


Output voltage standing wave ratio vs. frequency (Pin=-30dBm)



External Dimensions and Pressure Point Arrangement Diagram

External dimensions of HX116790C-0820P8

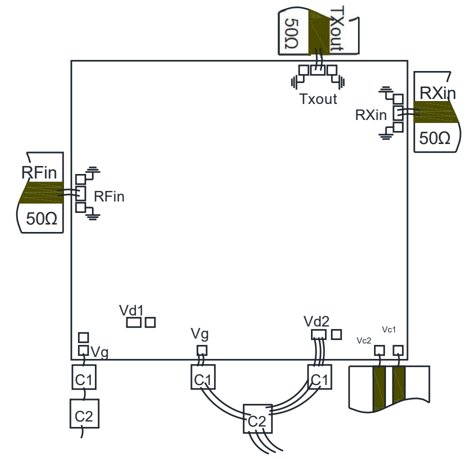


Note: All units in the figure are in micrometers (μm); dimensional tolerance ±100μm.

Pressure Point Arrangement Diagram

Serial number	Symbol	Function	Size
1	TXin	Emission input pressure point	100×150μm^2
2	TXout	Emission output pressure point	150×100μm^2
3	RXin	Gate bonding pressure point	100×150μm^2
4	Vc1	Switch control bonding pressure point 1	100×100μm^2
5	Vc2	Switch control bonding pressure point 2	100×100μm^2
6	Vd2	Drain bias voltage point 2	150×100μm^2
7	Vg	Gate bias voltage point	100×100μm^2
8	Vd1	Drain bias voltage point 1	150×100μm^2
9	Vg	Gate bias voltage point	100×100μm^2

Recommended Assembly Drawing



Note: 1) The capacitance values for peripheral capacitors are C1=100pF and C2=1000pF. Single-layer ceramic capacitors are recommended, with C1 positioned as close as possible to the chip and maintaining a distance of no more than 750μm.

2) For power circuits in the Ku-band and below, ceramic sintered microstrip lines with thicknesses of 200μm to 300μm can be fabricated on substrates to simplify assembly processes. For Ku-band and higher frequency bands, low-loss, low dielectric constant materials with thicknesses ranging from 125μm to 250μm are used for microstrip line bonding/sintering on substrates to reduce transmission loss, with input/output bonding wire lengths controlled within 350μm ± 150 μm.

Matters Need Attention

1） Single-chip circuits must be stored in a dry and clean nitrogen (N2) environment.

2） The chip substrate material 6H-SiC is highly brittle and must be handled with care to avoid damaging the chip.

3） The chip surface lacks an insulating protective layer, necessitating attention to the cleanliness of the assembly environment to prevent excessive surface contamination.

4） The thermal expansion coefficient of the carrier should be close to that of 6H-SiC, with a linear thermal expansion coefficient of 4.2×10^{-6}/℃. It is recommended to use CuMoCu or diamond/Cu as the carrier material.

5） During assembly, avoid gaps between the chip and the carrier while ensuring effective heat dissipation between the housing and the carrier.

6） It is recommended to use gold-silver solder for sintering with Au:Sn=80%:20%, where the sintering temperature should not exceed 300°C and the duration should not exceed 30 seconds. The sintering process must avoid rapid temperature fluctuations and requires gradual temperature rise and fall.

7） It is recommended to use gold wires with a diameter of 25μm to 30μm, maintain the temperature of the bonding platform base below 250°C, minimize bonding time, and avoid rapid temperature fluctuations during the bonding process.

8） During power-on, apply gate voltage before drain voltage; during power-off, first reduce drain voltage then gate voltage.

9） The chip incorporates DC-blocking capacitors for internal input/output, while its input terminals feature a DC-to-ground short-circuit configuration.

10）During chip usage and assembly, attention must be paid to anti-static measures, including wearing grounded anti-static wristbands and ensuring proper grounding of sintering and bonding platforms.

11）Please contact the supplier if you have any questions.

This product is sensitive to static electricity. Please take anti-static precautions during use.