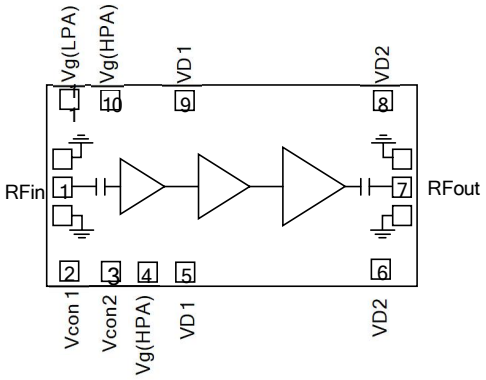
HX116532C-513P25 GaN MMIC **power amplifier chip,**5GHz～13GHz

Performance Features

- Frequency range: 5GHz to 13GHz
- Power gain: (Pulse) 5-7 GHz: 19 dB; 7-13 GHz: 21 dB (Continuous wave) 6 dB
- Maximum output power: (Pulse) 5-7 GHz: 43 dBm; 7-13 GHz: 45 dBm (Continuous wave): 30 dBm
- Additional efficiency: 35% (pulse) 10% (continuous wave)
- Pulse: +28V@2000mA (static)
- Continuous wave: +28V@130mA (static)
- Chip dimensions: 3.50mm × 4.20mm × 0.08mm

functional block diagram



Product Overview

The HX116532C-513P25 is a high-power amplifier chip implemented using GaN HEMT transistors, fabricated through a 0.25μm GaN power MMIC process. Capable of operating in both pulse and continuous wave modes, it covers a frequency range of 5GHz to 13GHz. In pulse mode, the power gain exceeds 19dB at 5-7GHz and 21dB at 7-13GHz, with a typical saturated output power of 25W and power add-on efficiency of 35%. Continuous wave operation delivers a power gain greater than 6dB, a typical saturated output power of 1W, and power add-on efficiency above 10%. The chip employs backside via grounding and dual power supply configuration, featuring typical operating voltages of Vd=+28V, $Vg_{(HPA)}$=-2.0V, and $Vg_{(LPA)}$=-5.0V. Primarily designed for microwave transceiver components and high-power solid-state transmitters, this chip demonstrates exceptional performance in diverse applications.

Microwave electrical parameters (TA = +25°C, Vd = +28V)

Metric	Symbol	Least value	Representative value	Crest value	Unit
Frequency range	f		5～13		GHz
Pulse saturation output power	Psat	43	45		dBm
Continuous wave saturated output power	Psat	30	32		dBm
Pulse power gain	Gp	19	21		dB
Continuous wave power gain	Gp	6	8		dB
Pulse Power Gain Flatness	△Gp			±1.5	dB
Continuous Wave Power Gain Flatness	△Gp			±1.6	dB
Pulse power added efficiency	PAE	30	35		%
Continuous wave power additive efficiency	PAE	10	15		%
Pulse linear gain	Gain		32	35	dB
Continuous wave linear gain	Gain		25	30	dB
Pulse Linear Gain Flatness	△Gain			±3	dB
Linearity gain flatness of continuous wave	△Gain			±5	dB
Pulse input standing wave	VSWR(in)		1.6	2	-
Standing wave with continuous wave input	VSWR(in)		2	2.6	-

Note: 1) All chips have undergone in-chip 100% DC testing and 100% RF testing.

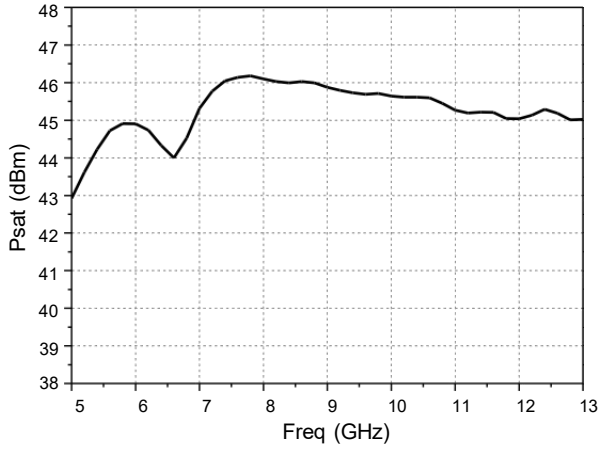
Limit usage parameters

Parameter	Symbol	Limit value
Maximum drain-source forward bias voltage	Vd	+35V
Minimum gate-source negative bias	Vg	-5V
Maximum input power	Pin	+28dBm
End-use temperature	T_{op}	-55℃~+85℃
Storage temperature	T_{STG}	-65℃~+150℃

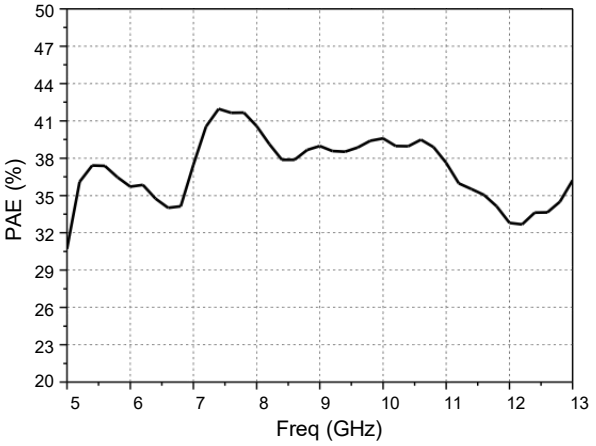
Representative Set of Curves

1、 Pulse test data (Vd=+28V, VG(HPA)=-2.0V, VG(LPA)=-5.0V, Vcon1=0V, Vcon2=-25V)

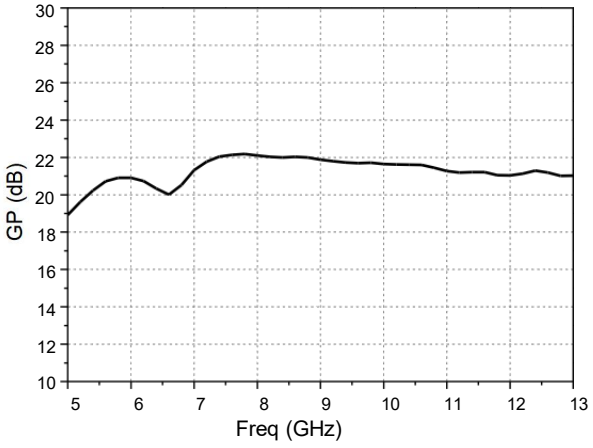
Maximum output power vs. frequency (Pin=24dBm)



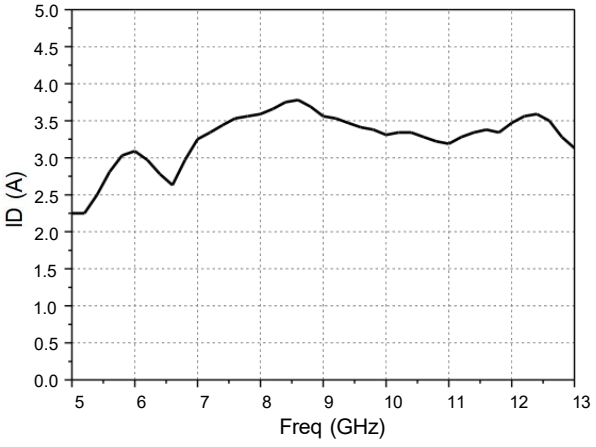
Additional efficiency vs. frequency (Pin=24dBm)



Power gain vs. frequency (Pin=24dBm)

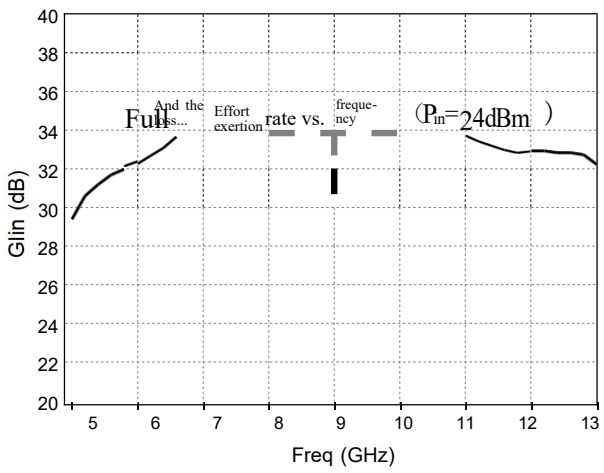


Drain dynamic current vs. frequency (Pin=24dBm)

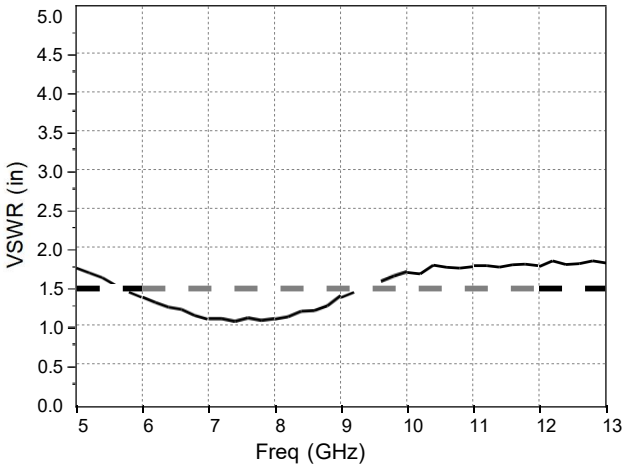


2、Continuous wave test data (Vd=+28V，

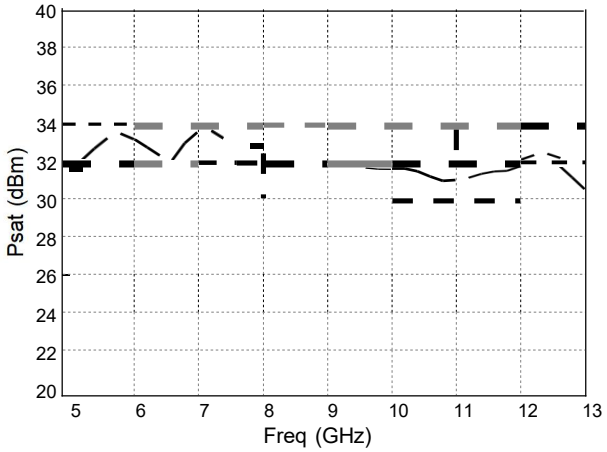
Enter standing wave vs. frequency (Pin=-30dBm)



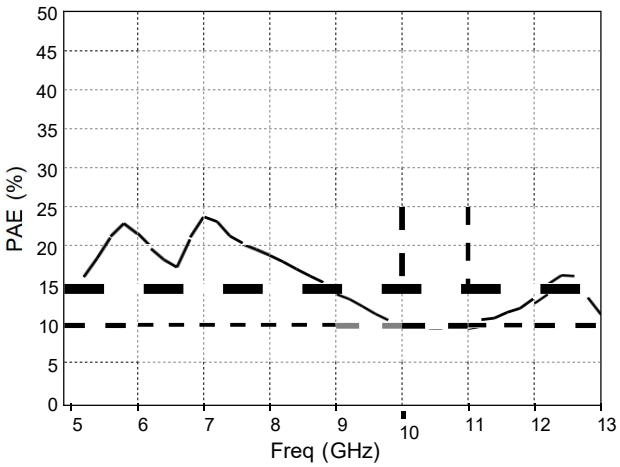
Enter standing wave vs. frequency (Pin-30dBm)



$V_{G(HPA)}$=-5.0V，$V_{G(LPA)}$=-2.0V，Vcon1=-25V，Vcon2=0V）

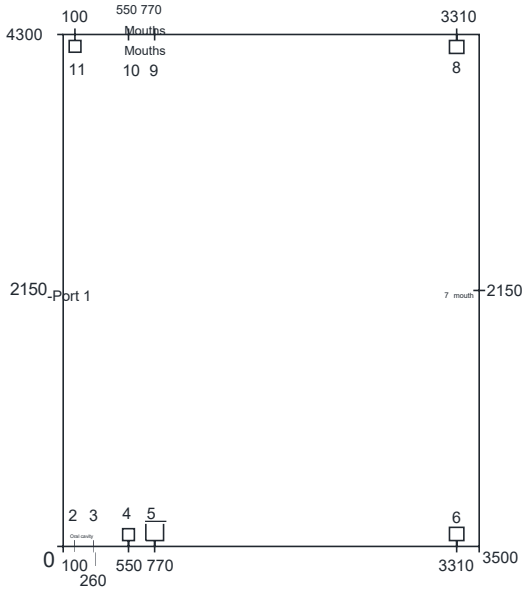


Additional efficiency vs. frequency (Pin=24dBm)



External dimensions and pressure point arrangement diagram

External dimensions of HX116532C-513P25



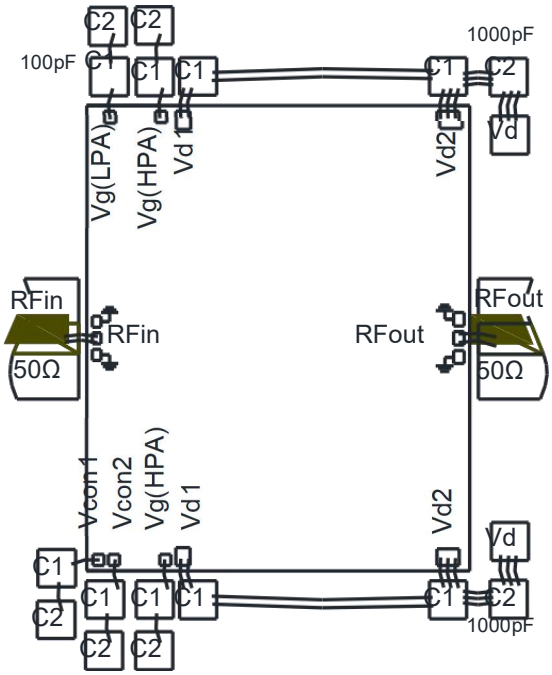
Note: All units in the figure are micrometers (μm).

The dimensional tolerance is ± 100 μm.

Pressure Point Arrangement Diagram

Serial number	Symbol	Function	Size
1	RFin	Radio frequency input signal point	100×120μm²
2	Vcon1	Switch control 1 bonding point	100×100μm²
3	Vcon2	Switch control 2 bonding point	94×100μm²
4	$V_{G(HPA)}$	HPA grid bias bonding point	100×100μm²
5	V_{D1}	First-order level-biased bonding point	150×140μm²
6	V_{D2}	Second-order level-biased bonding point	120×110μm²
7	RFout	Radio frequency output signal point	100×120μm²
8	V_{D1}	Second-order level-biased bonding point	120×110μm²
9	V_{D2}	First-order level-biased bonding point	150×140μm²
10	$V_{G(HPA)}$	HPA grid bias bonding point	100×100μm²
11	$V_{G(LPA)}$	LPA gate bias bonding point	100×100μm²

Recommended assembly drawing



Note: The capacitance values for peripheral capacitor C1 and C2 are 100pF and 1000pF, respectively.

Matters Need Attention

1) For use in environmental purification systems;

2) GaN materials are brittle and their chip surfaces are highly susceptible to damage (avoid direct contact with the surface). Exercise caution during handling.

3) Use two bonding wires (25μm diameter gold wires) for input and output connections. The bonding wires should be as short as possible, not exceeding 300 μm in length.

4) The input and output are connected by a DC-blocking capacitor.

5) Use 80/20 gold-tin solder for sintering. The sintering temperature should not exceed 300°C, and the sintering time should be as short as possible, not exceeding 30 seconds.

6) This product belongs to electrostatic-sensitive devices. Prevent static electricity during storage and use.

7) Store in a dry, nitrogen atmosphere;

8) Do not attempt to clean the chip surface using dry or wet chemical methods;

9) Please contact the supplier if you have any questions.

This product is sensitive to static electricity. Please take anti-static precautions during use.